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MS-7830

m-ATX

Ver: 1.1 (243.84 * 243.84)

Intel Sharkbay plamform B85 colay H81

CPU:

INTEL-Haswell LGA1150

System Chipset:

INTEL-LYNX

Memory:

DDRIII (1333/1666MHz) * 4 (Dual Channel)

PWM:

VRD12 - ISL95812 + ISL6208

Other:

DVI * 1
VGA * 1
HDMI * 1

OnBoard Chipset:

HD Audio Codec: ALC887 (type B)
LAN: RTL8111G colay Dash
SIO: Nuvoton 6779
SPI ROM: B85-128M colay H81-64M

B85:

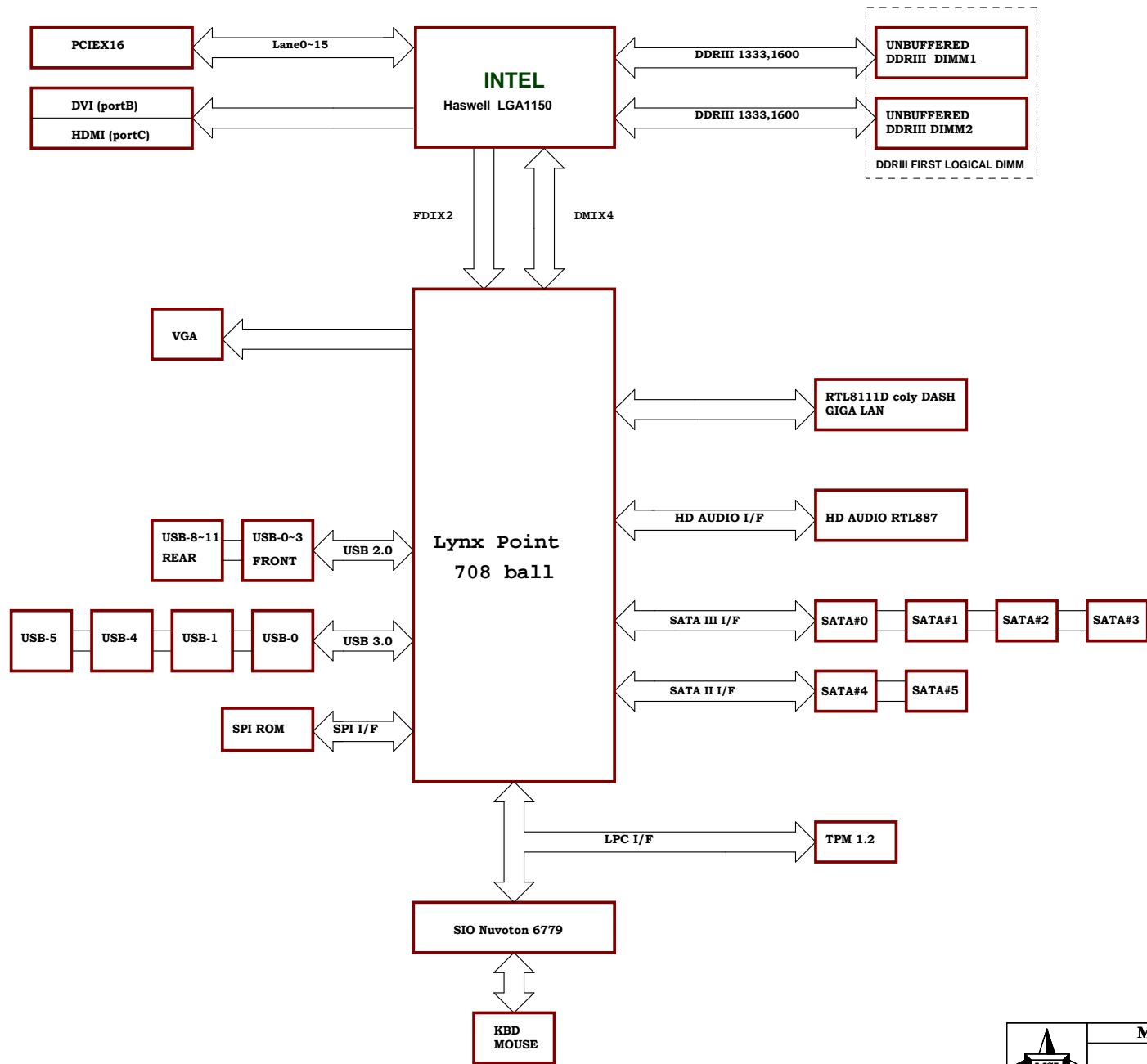
SATA2 * 2
SATA3 * 4
FRONT USB2.0 * 4
REAL USB2.0 * 4
FRONT USB3.0 * 2
REAL USB3.0 * 2

H81:

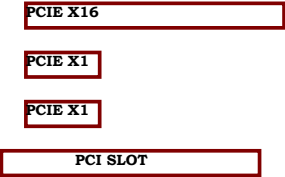
SATA2 * 2
SATA3 * 2
FRONT USB2.0 * 4
REAL USB2.0 * 4
REAL USB3.0 * 2

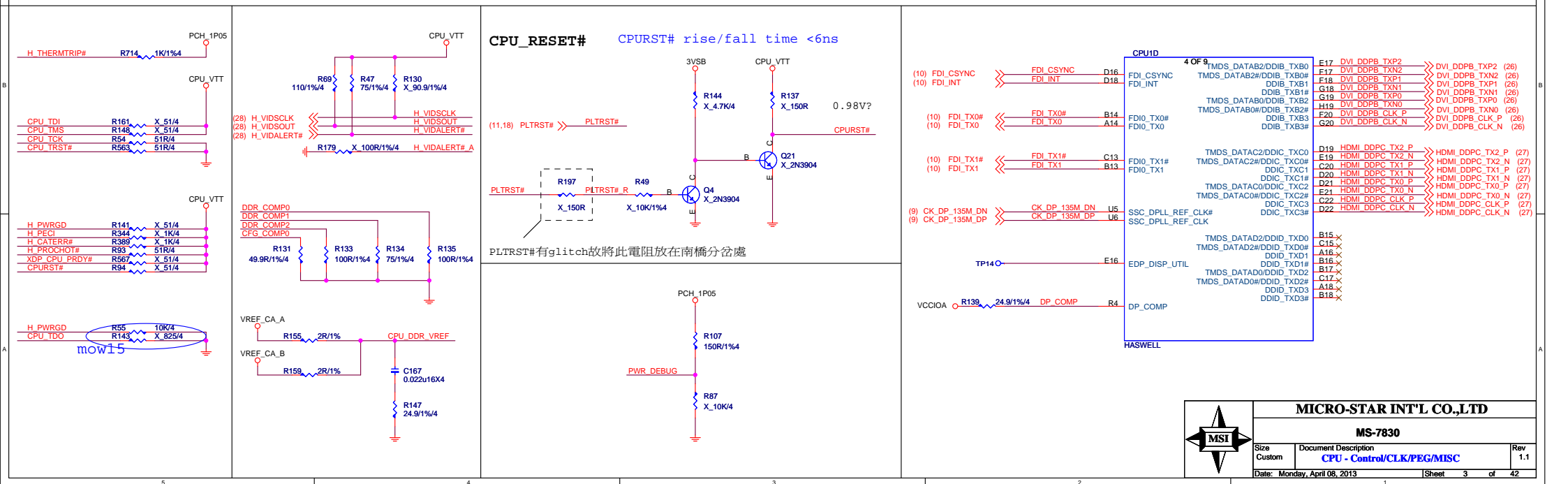
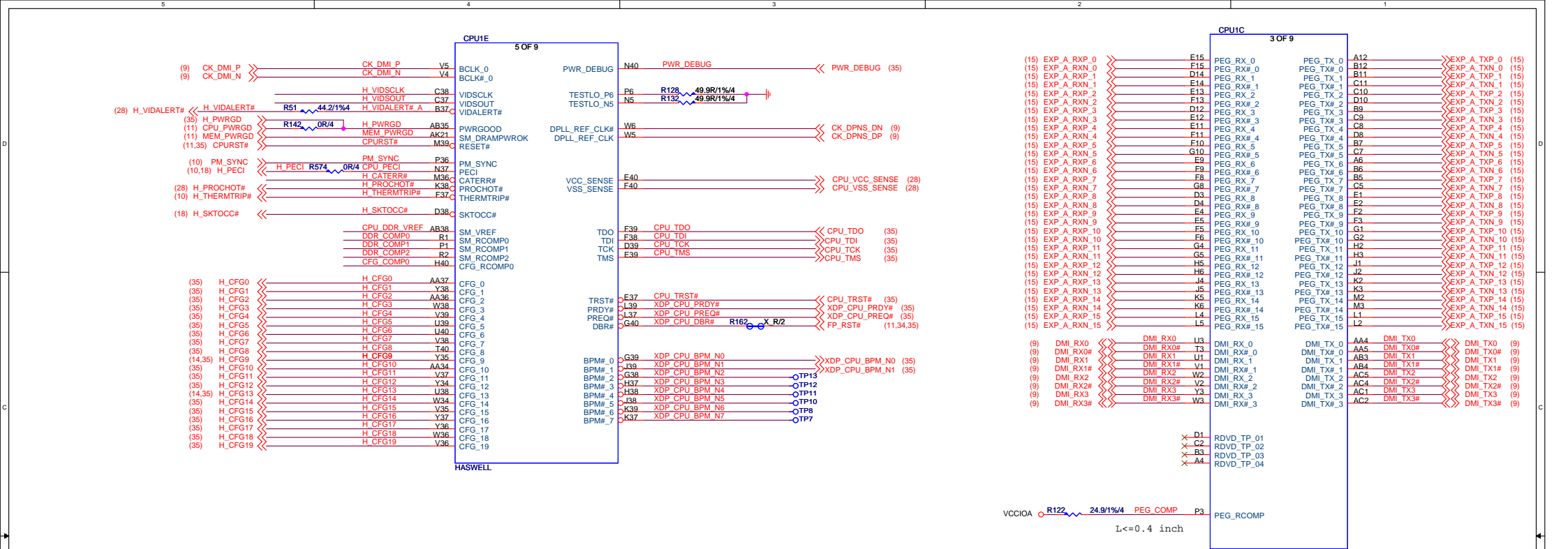
Expansion Slots:

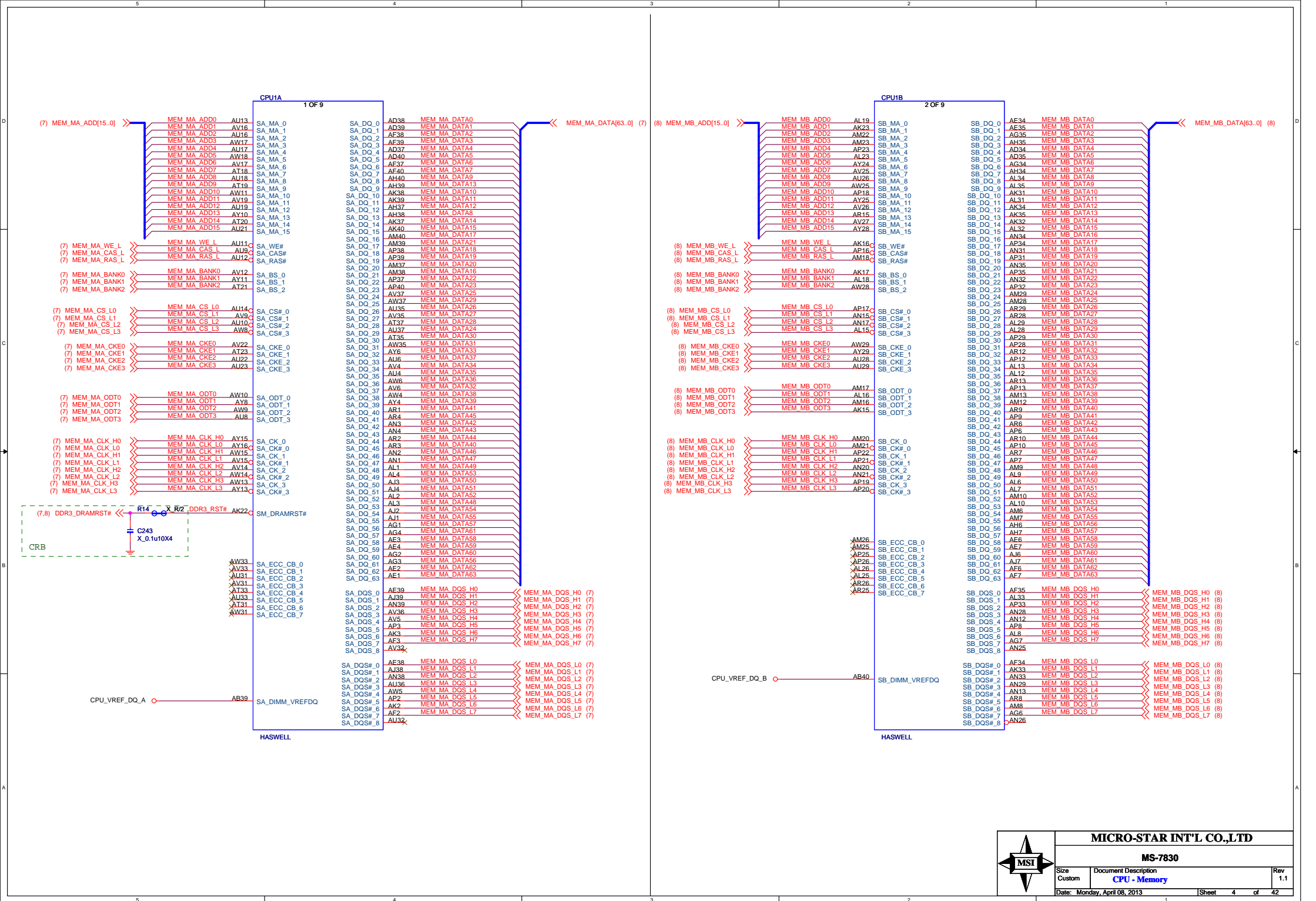
PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot * 1

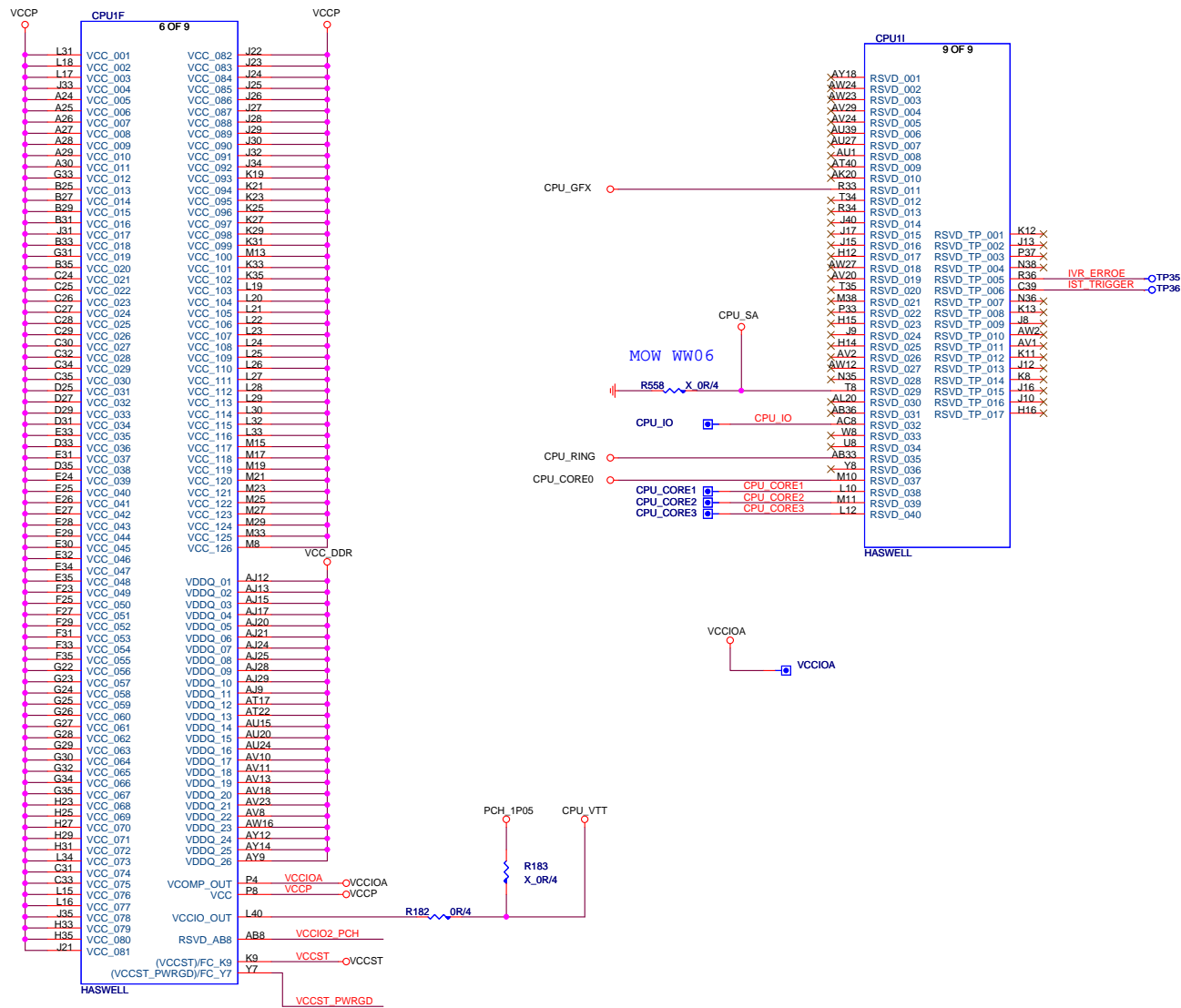


Slot Sequence:

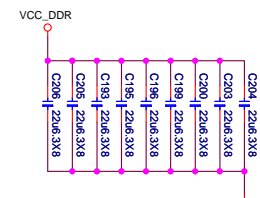






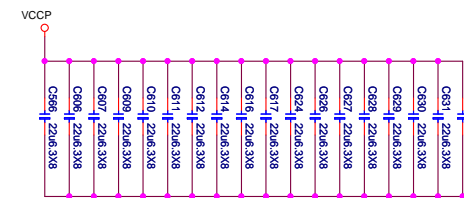


+1.5V_DDR3-Decoupling



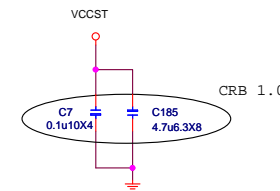
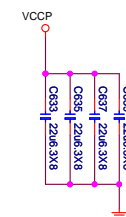
CPU SOCKET CAVITY 0805CAPS

+CPU_VCCP-Decoupling



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

PLACE 0805CAPS Near CPU SOCKET edge



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GND

GND



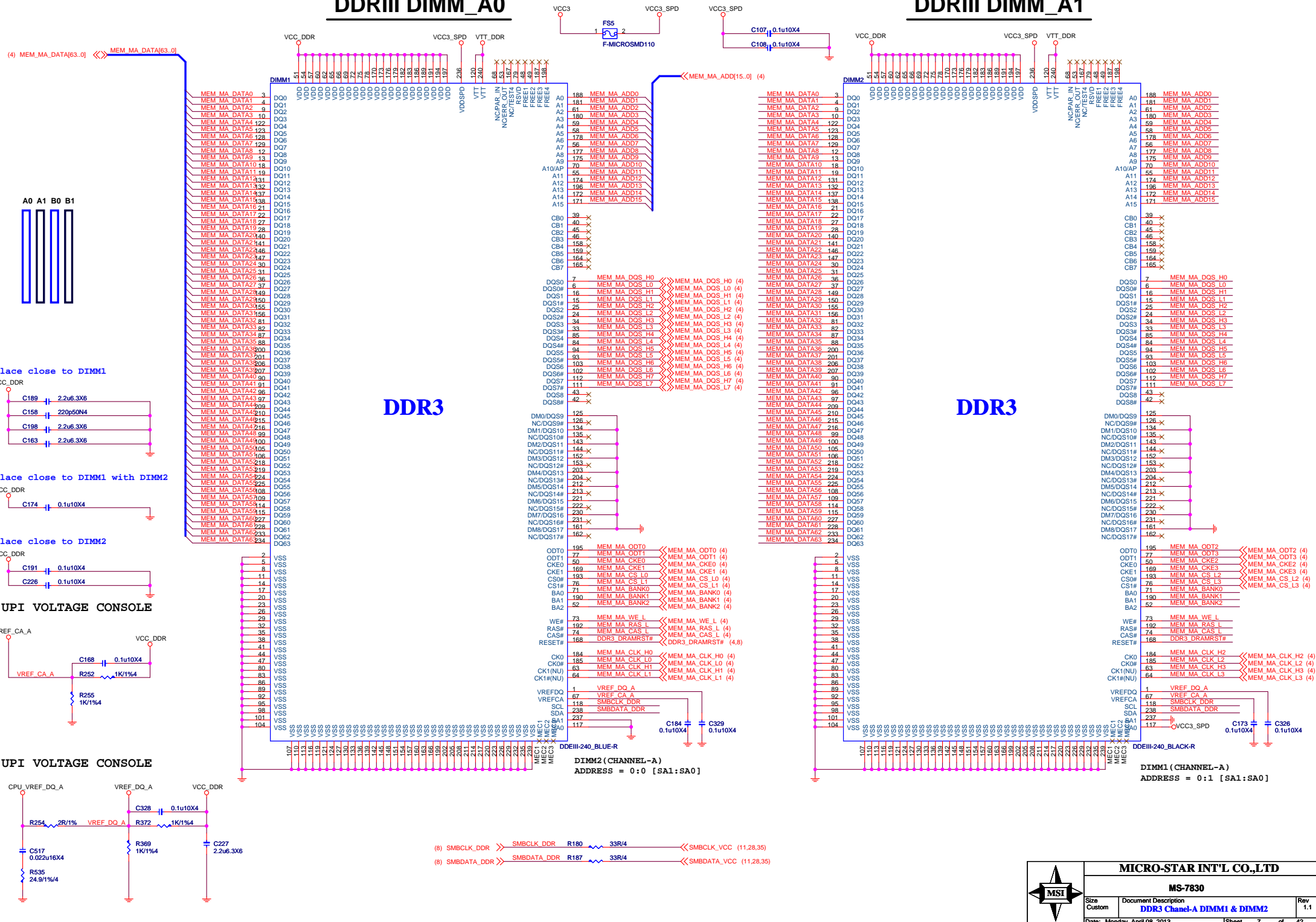
MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU - GND	1.1
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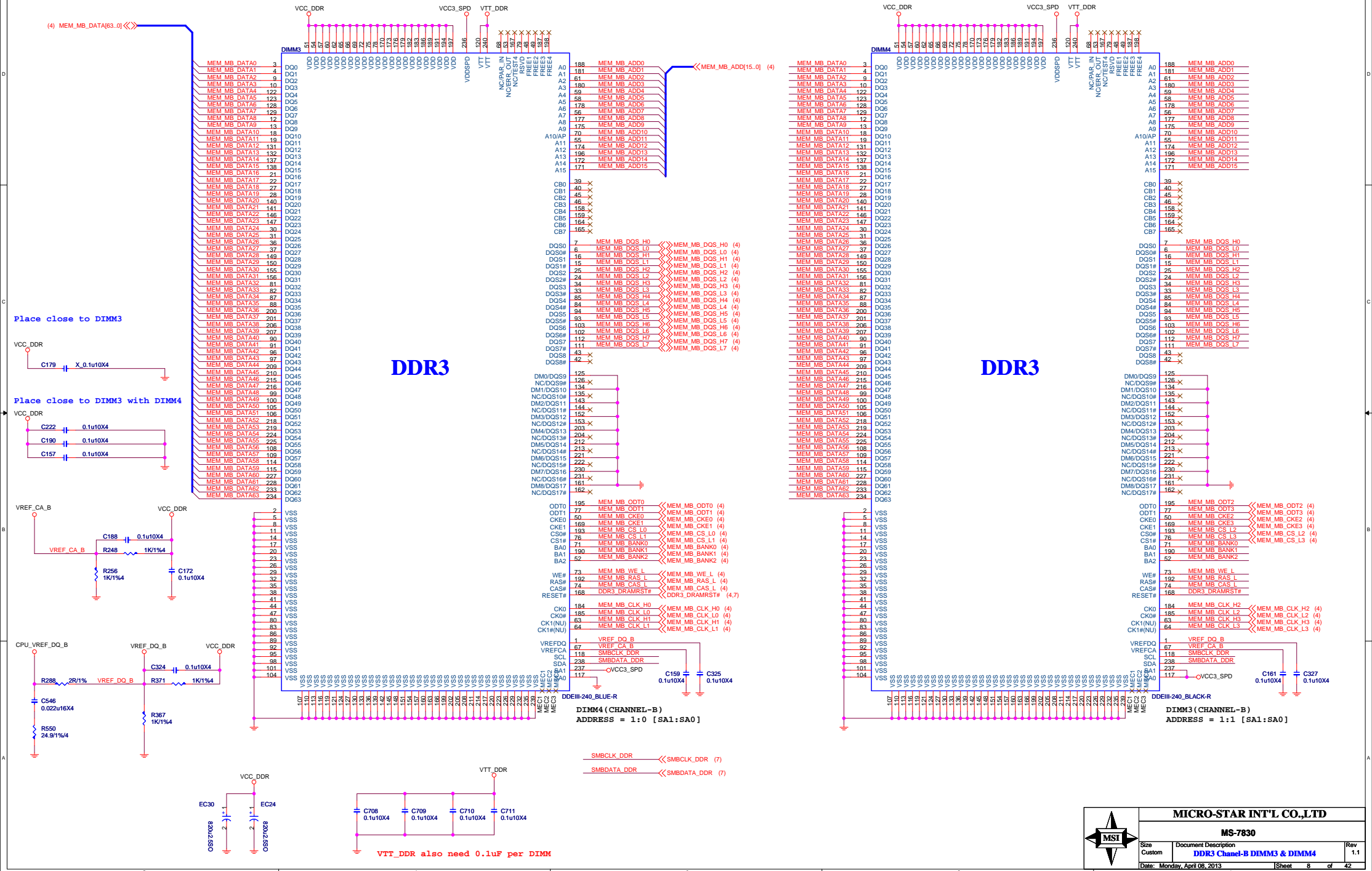
DDRIII DIMM_A0

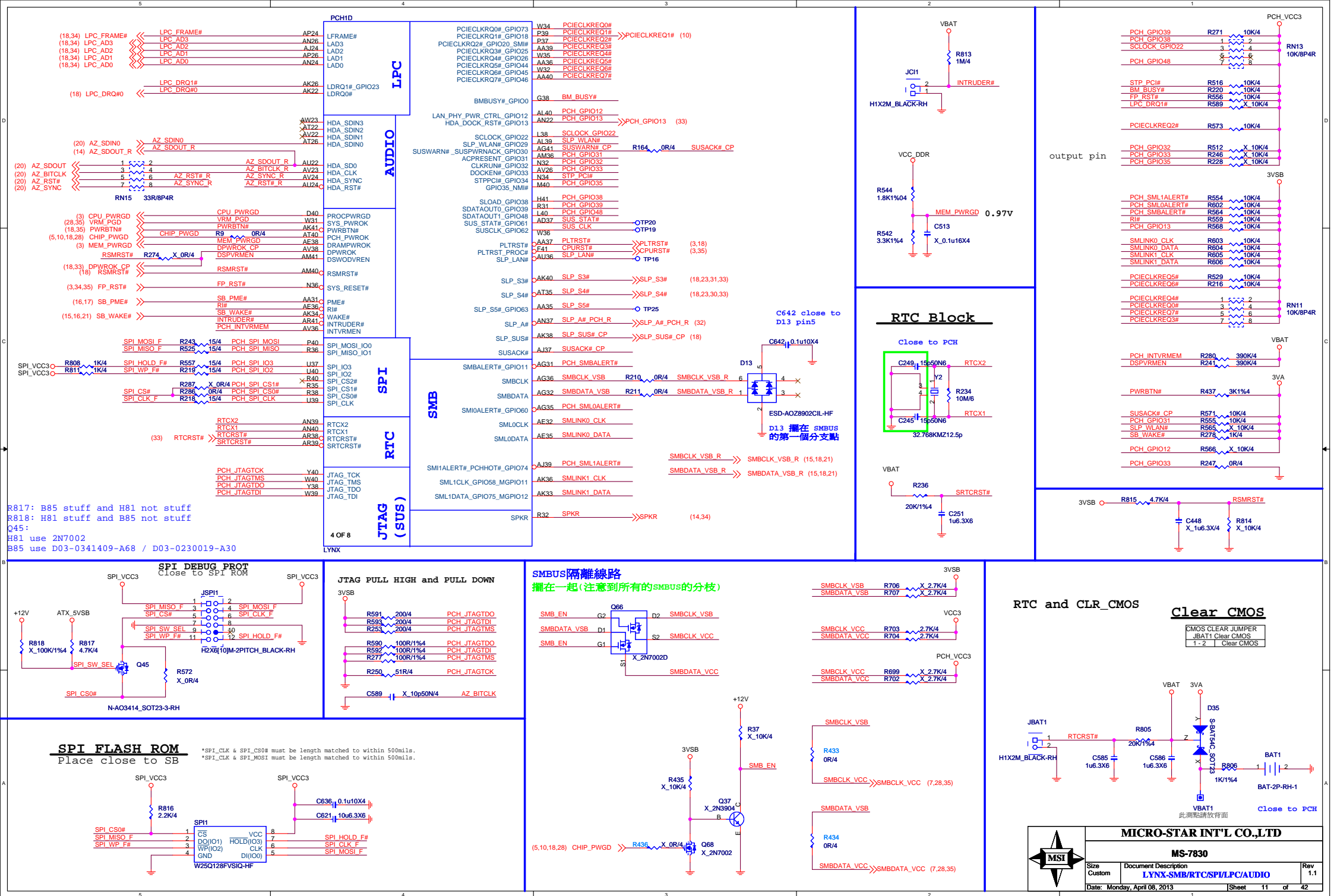
DDRIII DIMM_A1



DDRIII DIMM_B0

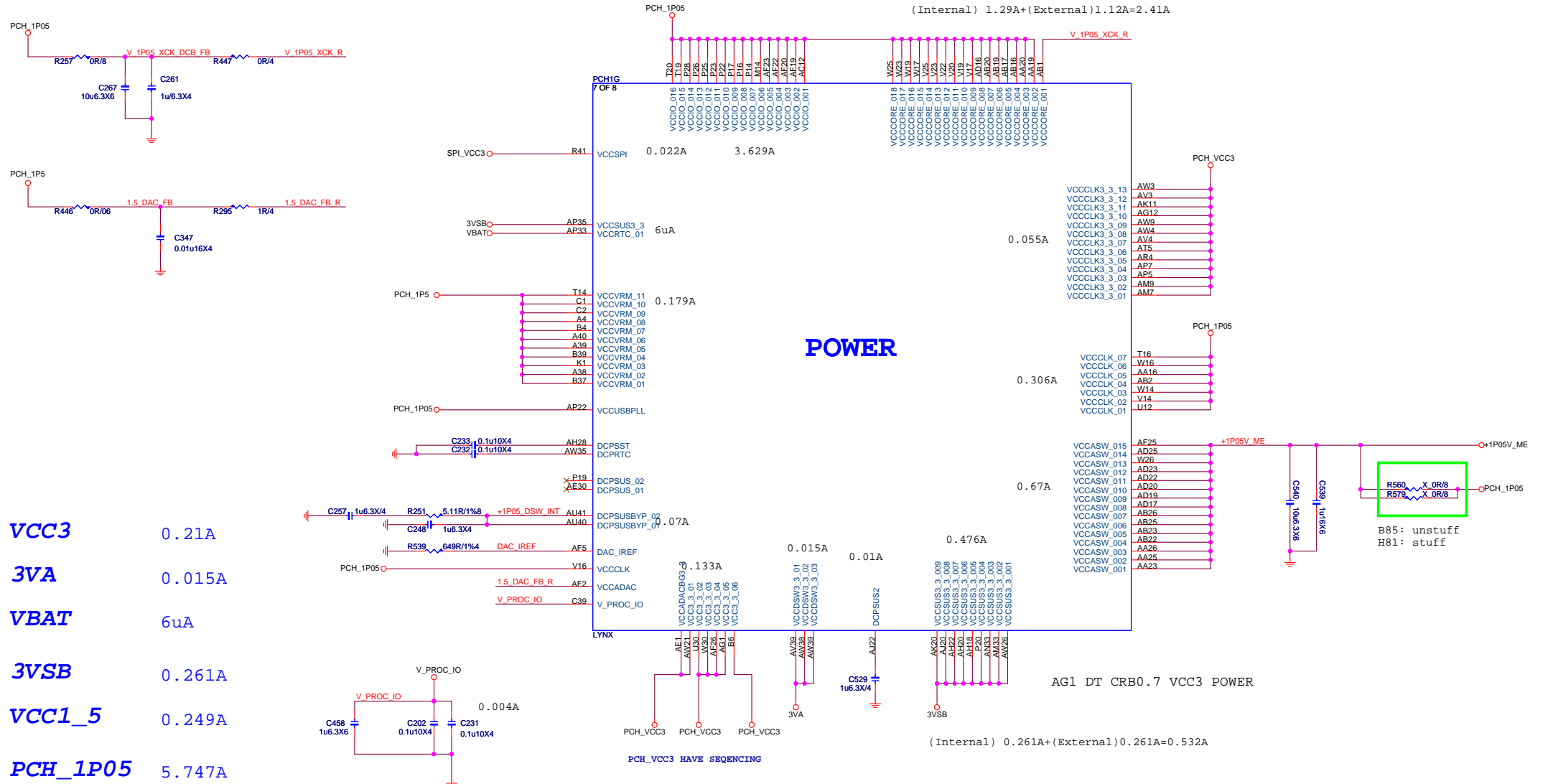
DDRIII DIMM_B1





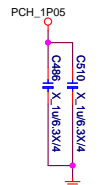
Change to 100H if
VCCA_DPLL/VCCA_DPLL
has noise issue.

AF25 ;AD25 DT CRB0.7 ASW POWER

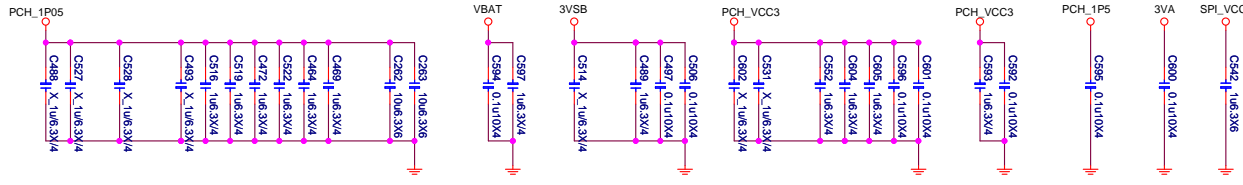


Backside for
U12,V14,
T16,V16
near U12 & V16

unstuff



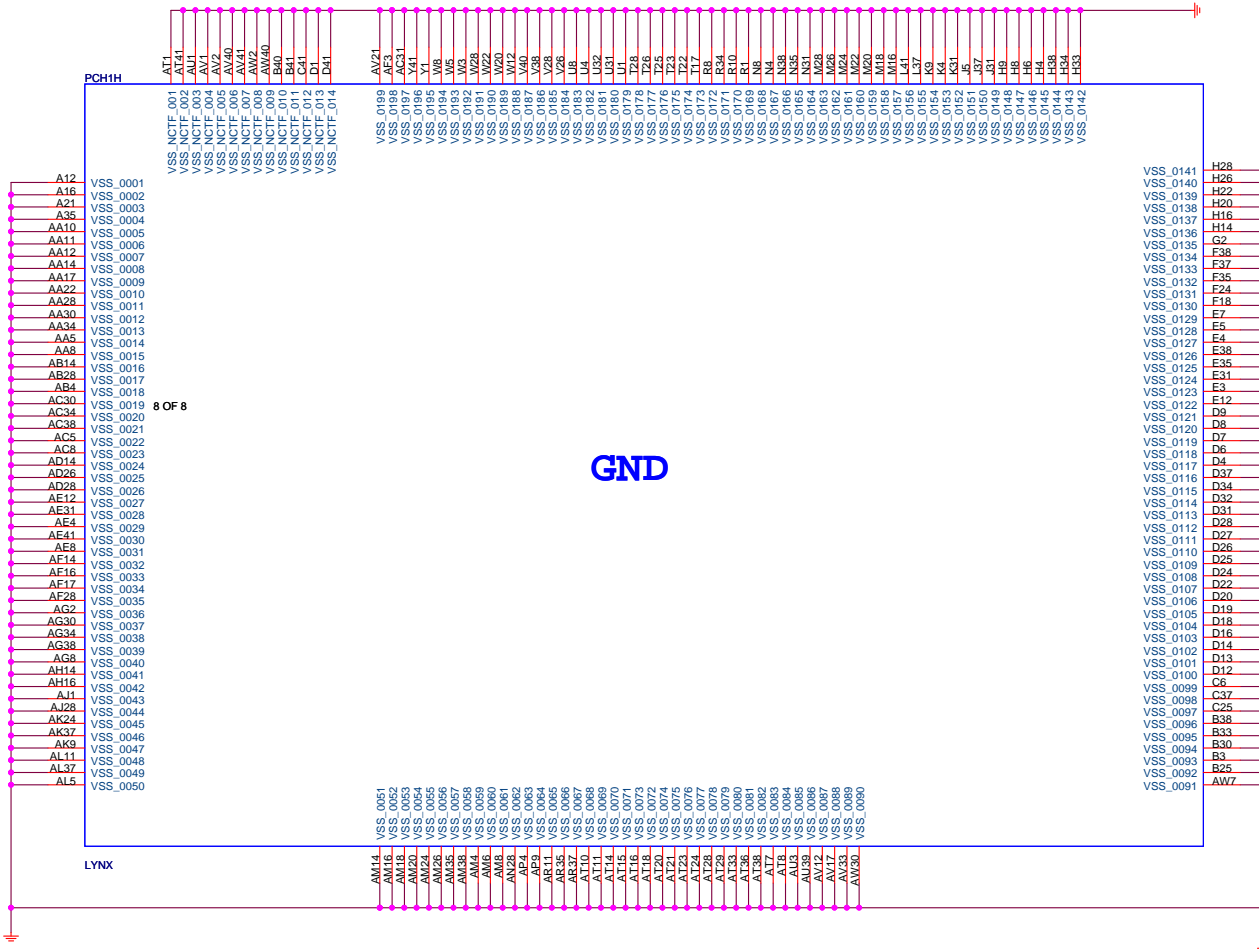
PCH decoupling cap



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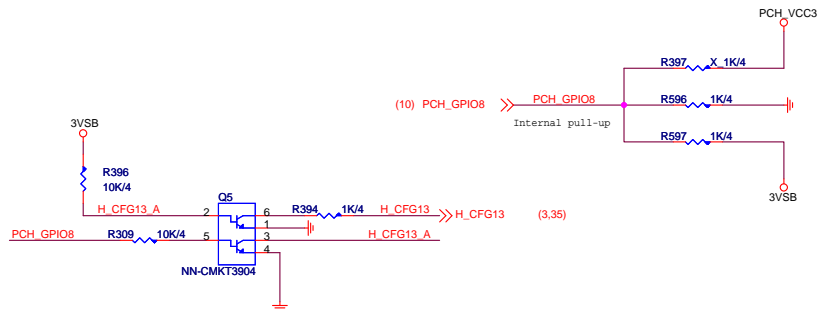
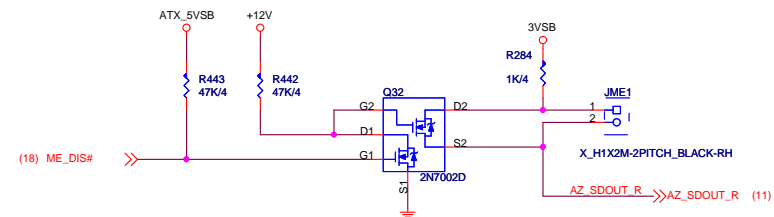
(11,34) SPKR << SPKR R538 X 8.2K/4 PCH_VCC3

Internal pull-DOWN

SPKR
Default Mode:
Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.

刷ME解锁

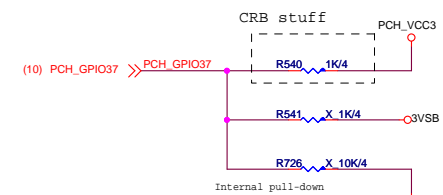


(10) PCH_GPIO55 >> PCH_GPIO55 R543 X 4.7K/4

Internal pull-up

GPIO55
Default Mode:
Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

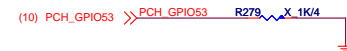


Enable TLS:
Pull up with 1k Ohm to VccSus3.3.

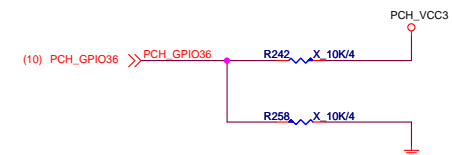
Default (Disable TLS):
Leave NC. Internal pull down.



For Sx power Cycling May Fail Due to SVID Logic Race Condition Within the Processor



GPIO53
Connect to ground with 1k Ohm pull-down resistor.



Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

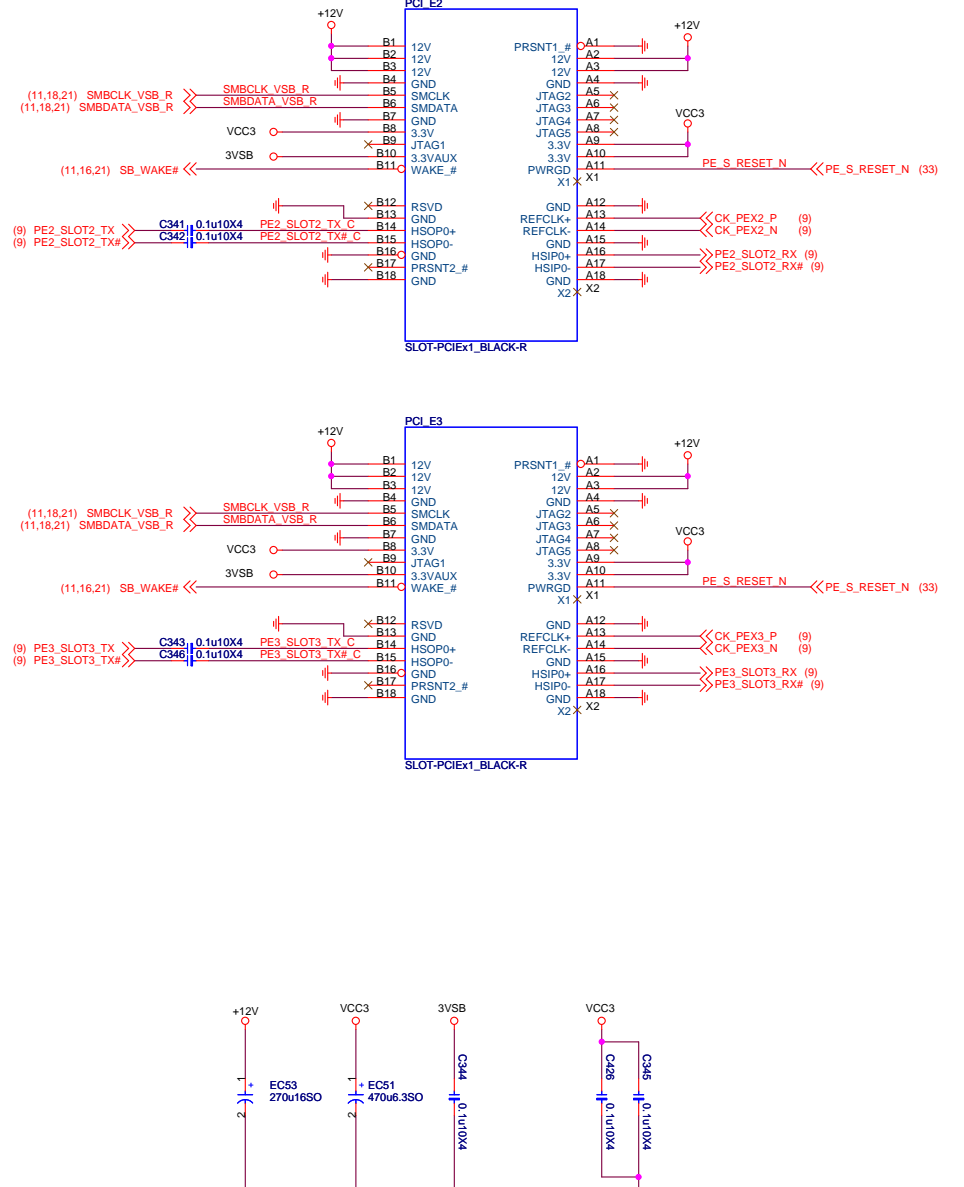
Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

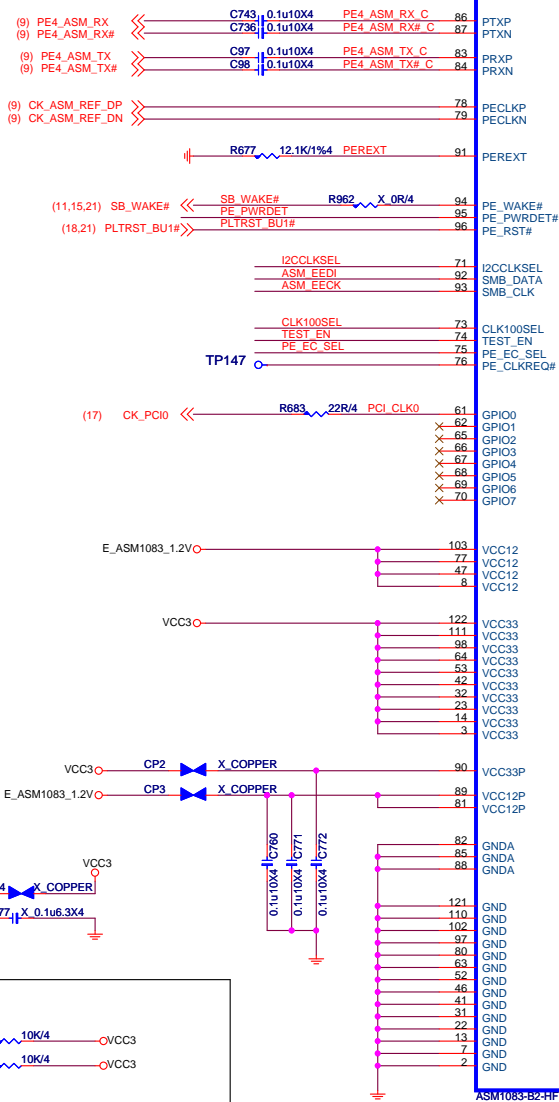
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default



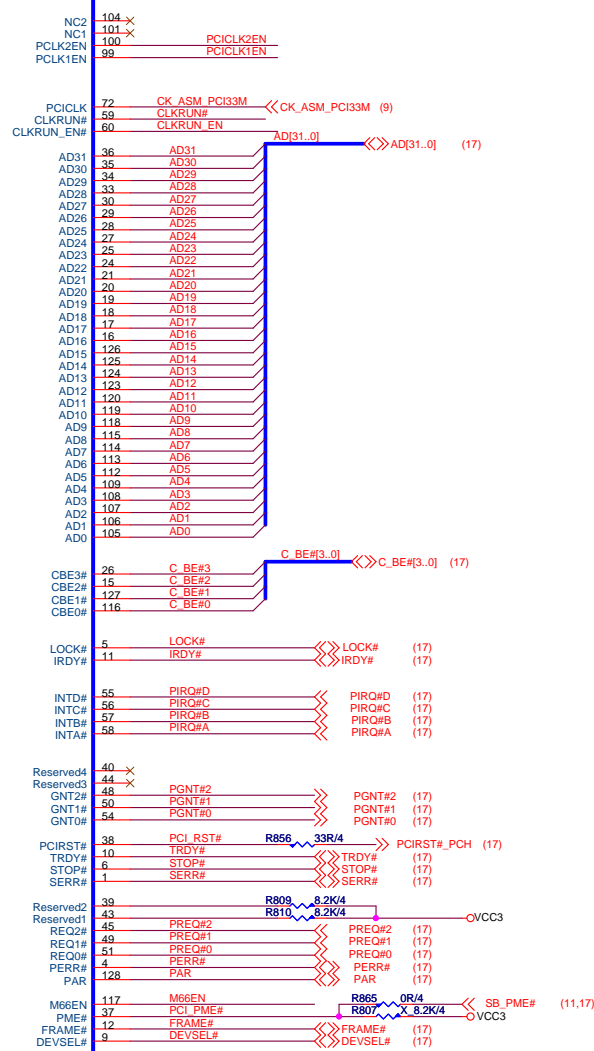
MICRO-STAR INT'L CO.,LTD		
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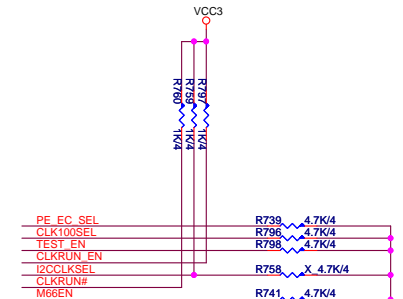


ASM1083

ASM1083-B2-HF



H/W Strapping



PE_EC_SEL-
 "H" for Express Card mode
 "L" for PCIe Riser Card mode

CLK100SEL-
 "H" for PECLK input only
 "L" for PECLK & PCICLK input

TEST_EN-
 "H" for Test Mode Enable
 "L" for Test Mode Disable

CLKRUN_EN-
 "H" for CLKRUN Mode Disable
 "L" for CLKRUN Mode Enable

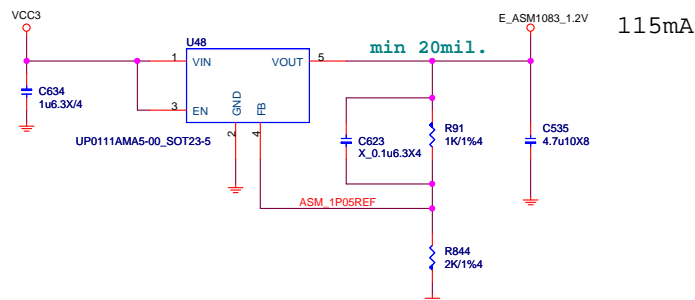
I2CCLKSEL-
 "H" is 135KHz I2CCLK
 "L" is 67.5KHz I2CCLK



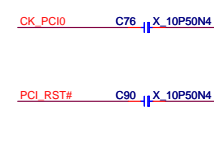
MICRO-STAR INT'L CO.,LTD

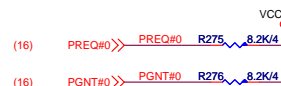
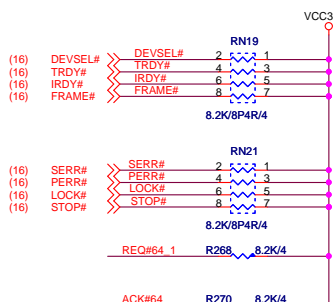
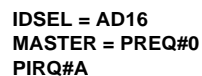
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EMI





PCI slot (X3)		
+3.3Vaux	(wake)	- 750mA
+3.3Vaux	(no wake)	- 40mA
+3.3V		- 7.6A
+5V		- 10A
+12V		- 1A

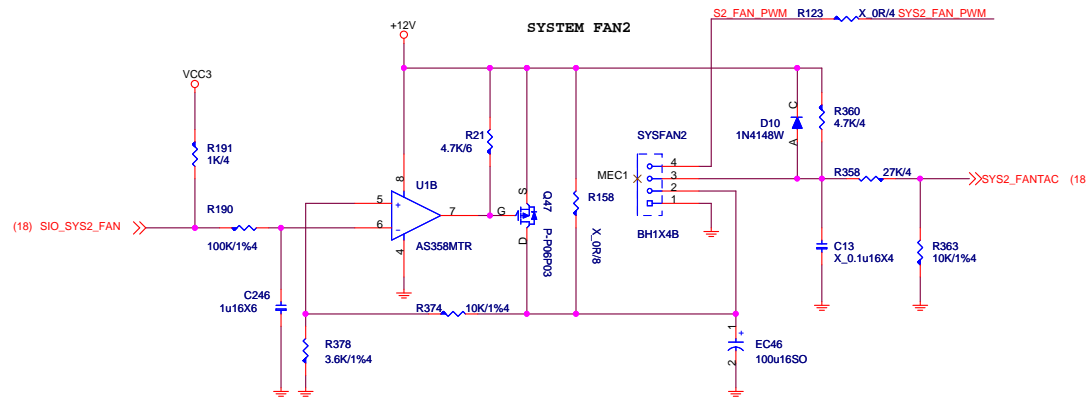
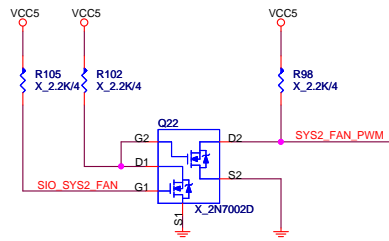
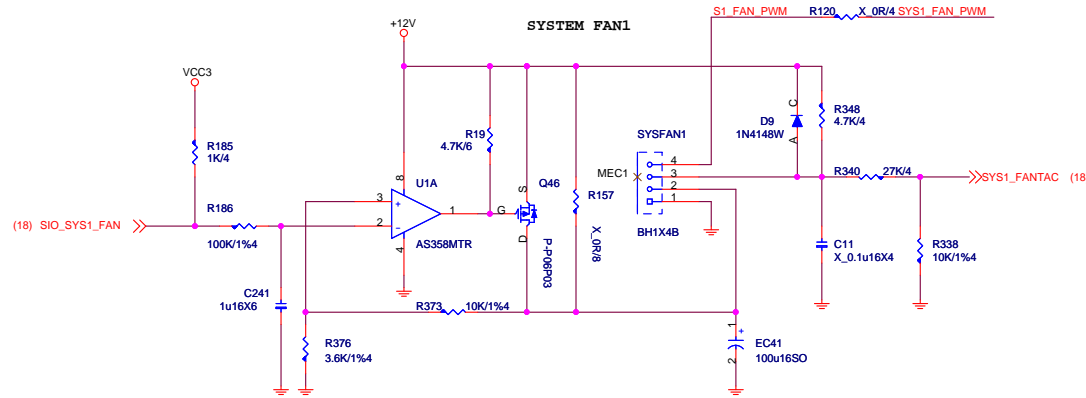
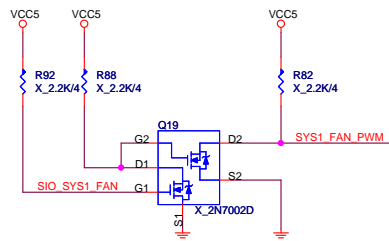
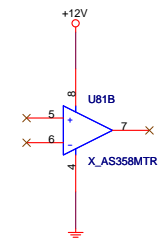
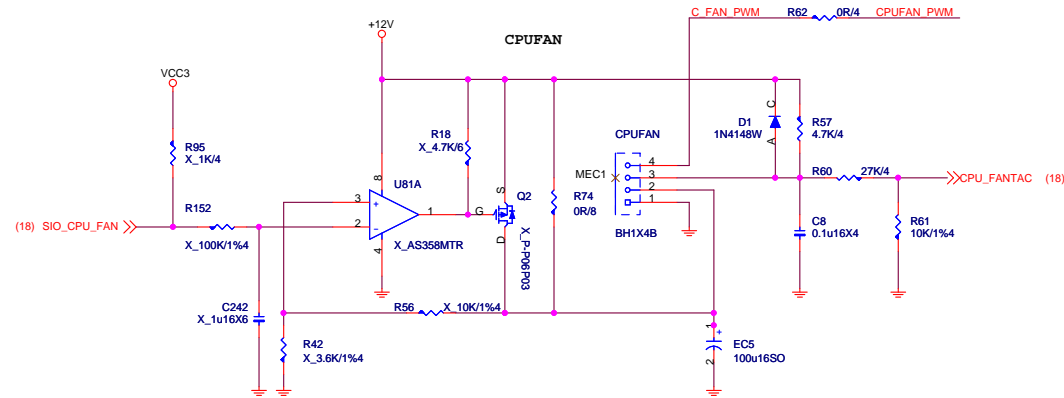
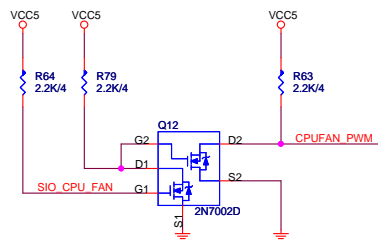


MICRO-STAR INT'L CO.,LTD

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FAN-COUNTROL CIRCUIT

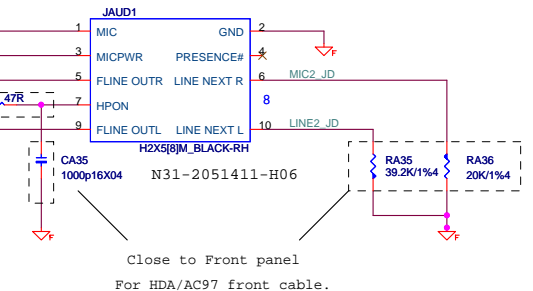
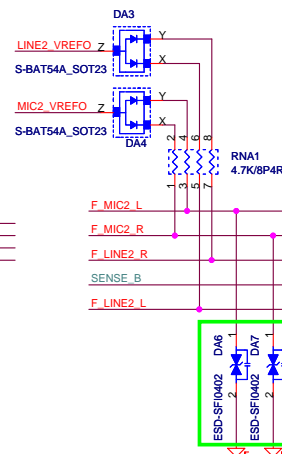
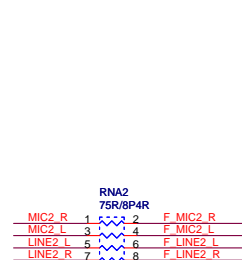
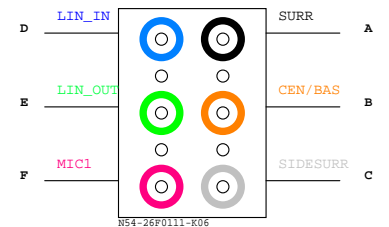
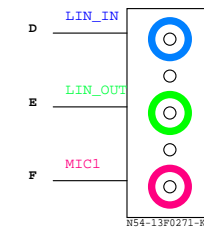
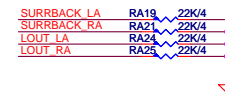
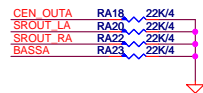
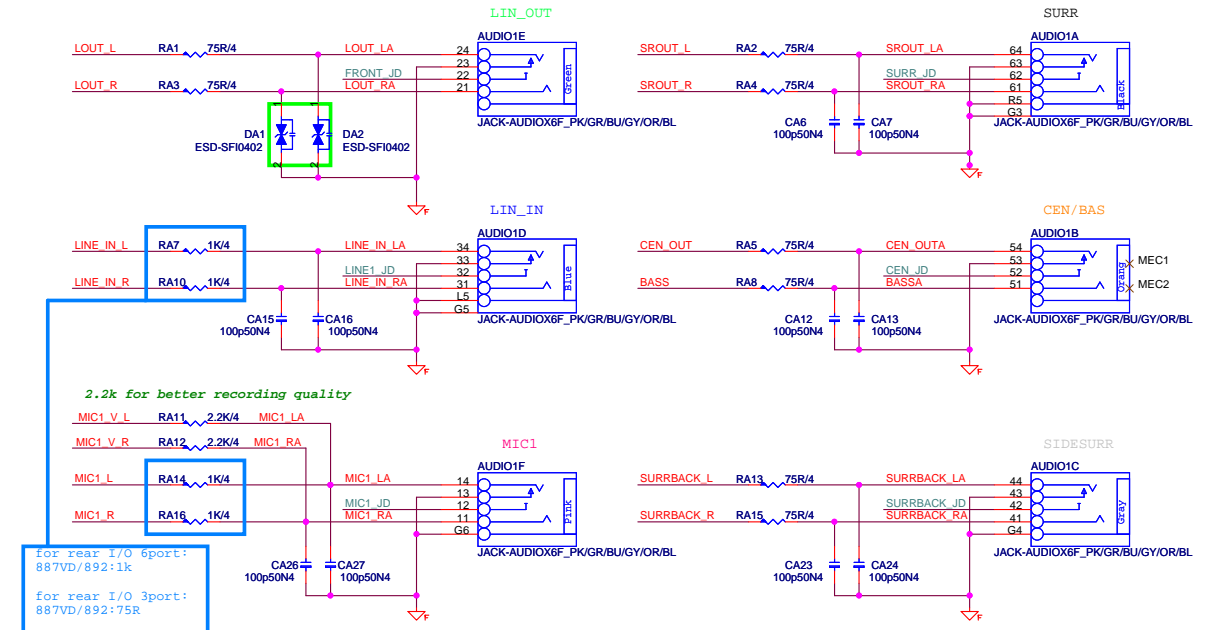
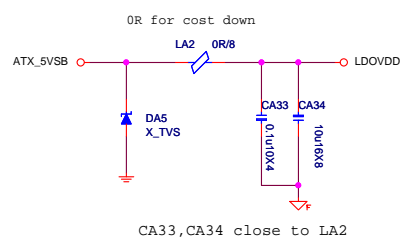
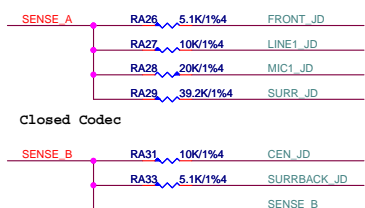
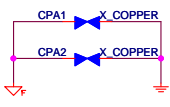
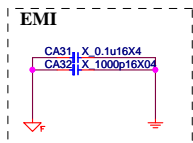
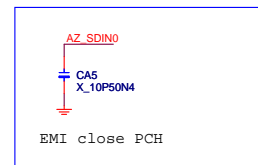
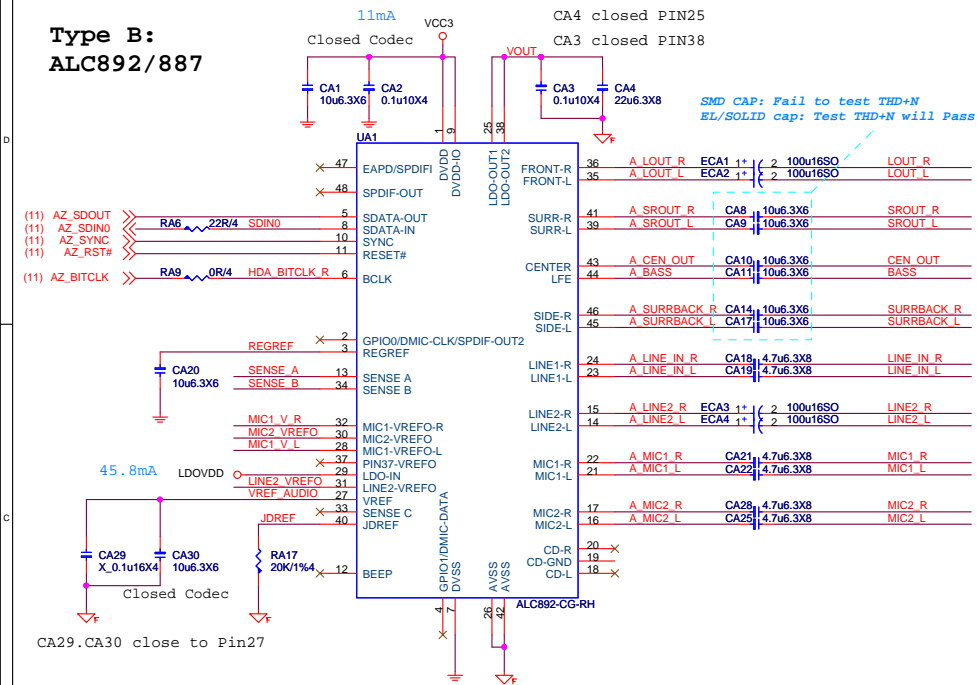


MICRO-STAR INT'L CO.,LTD

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Type B:
ALC892/887

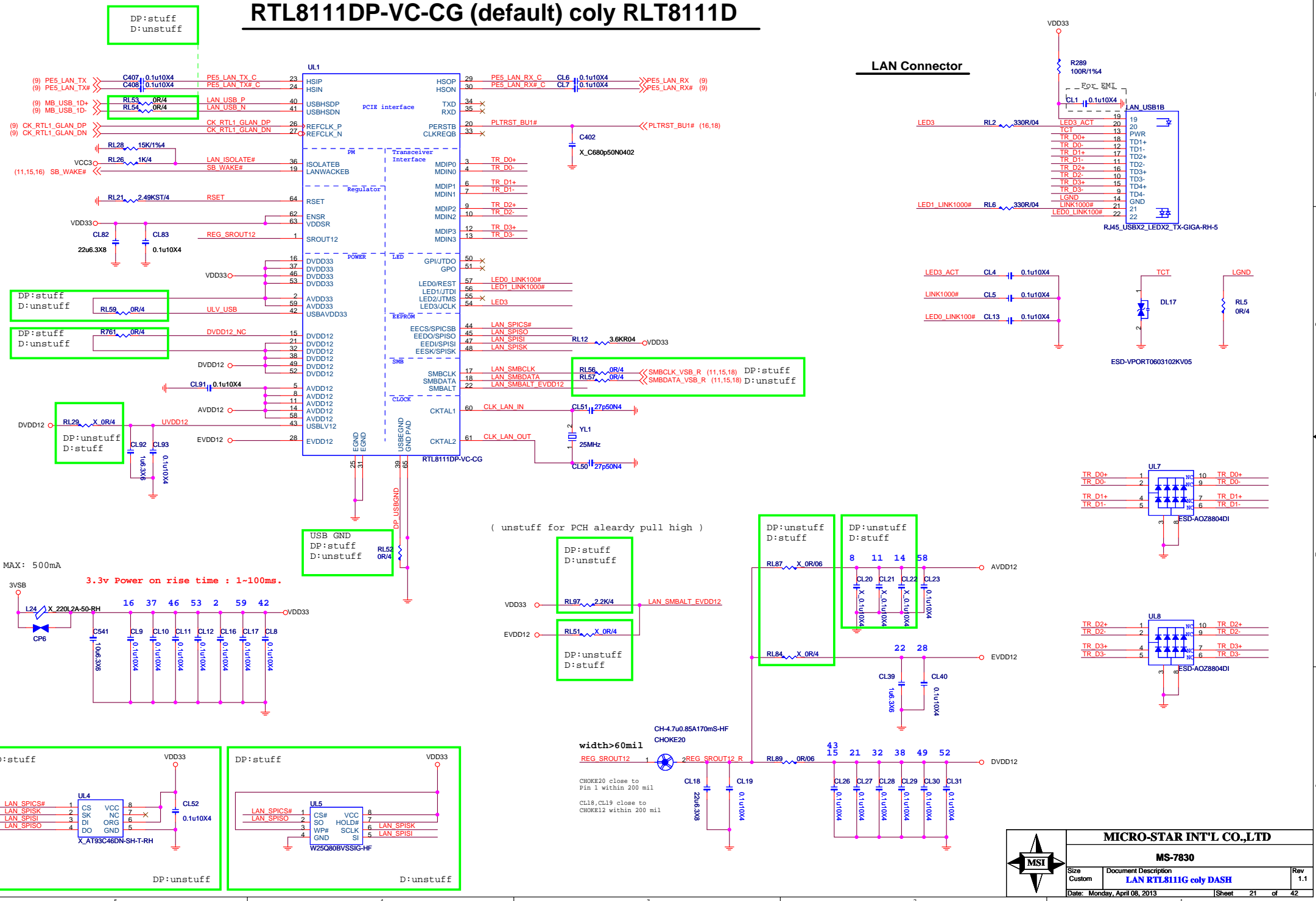


Varister --> cap for cost down
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack



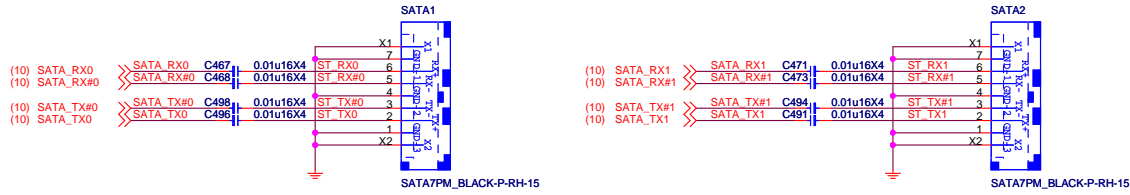
MICRO-STAR INT'L CO.,LTD			
MS-7830			
Size Custom	Document Description Audio Codec ALC887		Rev 1.1
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RTL8111DP-VC-CG (default) coly RLT8111D



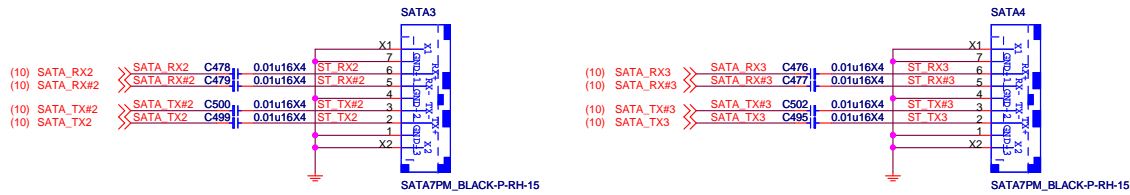
SATA 6G PORT 0,1

3.0 white 180 degree

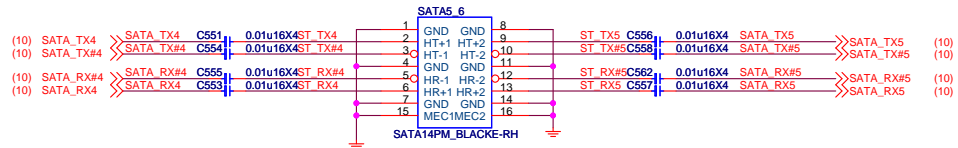


SATA 6G PORT 2,3

3.0 white 180 degree



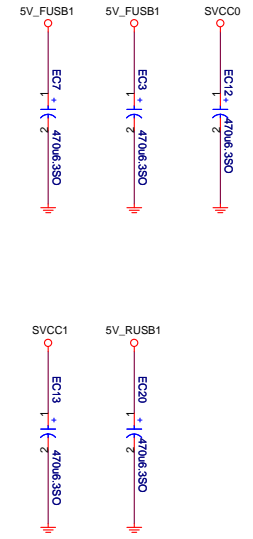
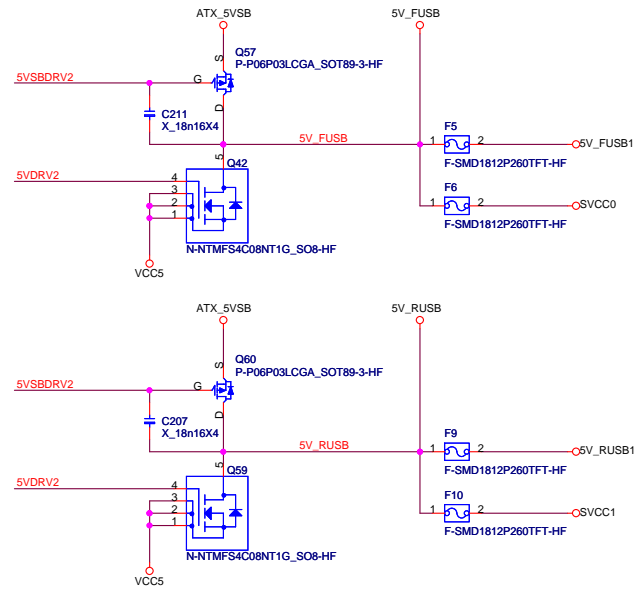
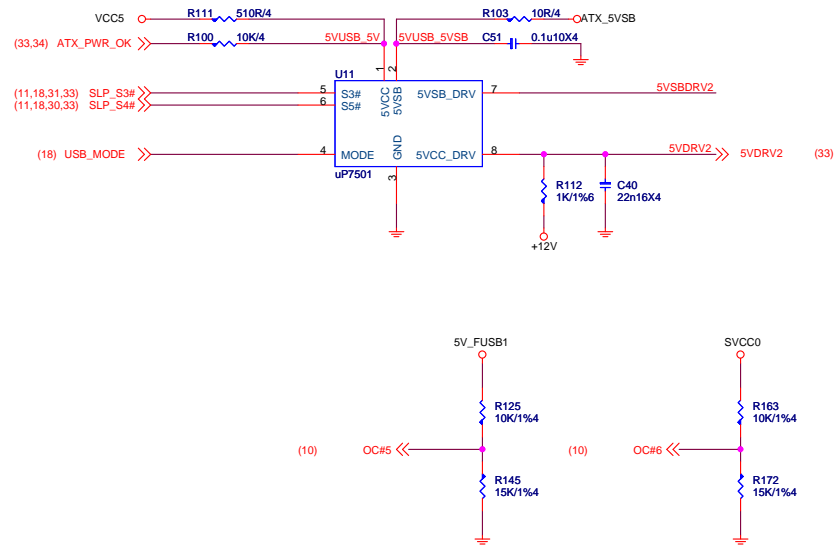
SATA 3G PORT 4,5



MICRO-STAR INT'L CO.,LTD

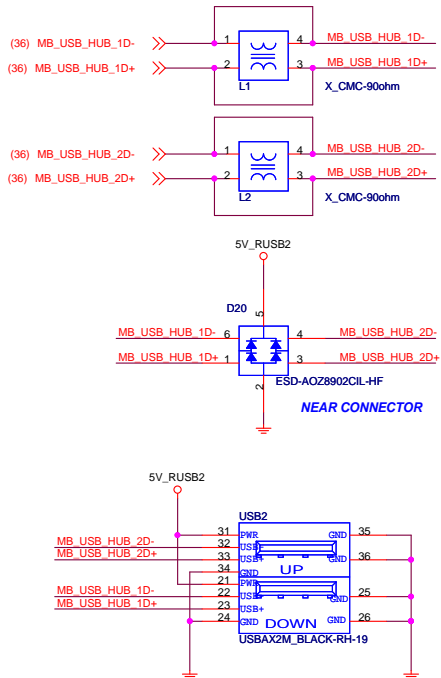
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Custom	SATA Connector	1.1
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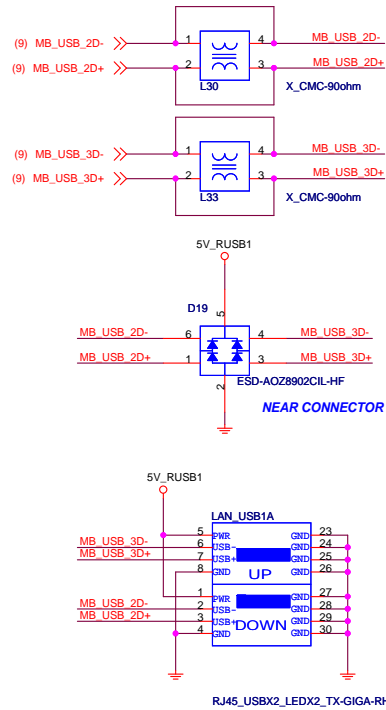


5VDRV1, 5VSBDRV1 width 12mil
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 2 USB ports

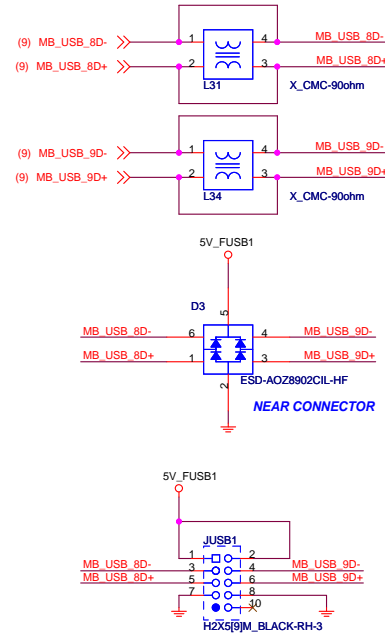
REAR USB PORT 2,3 (With PS2)



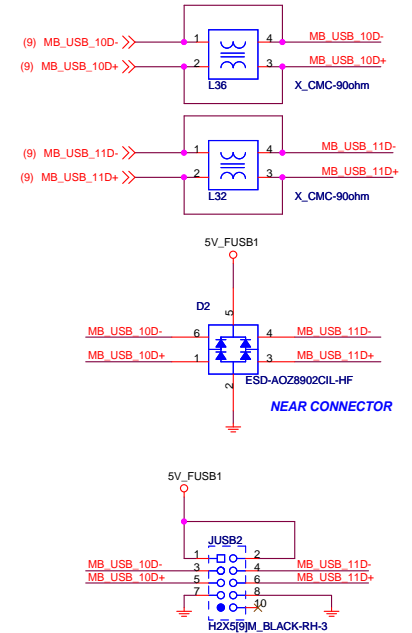
FRONT USB PORT 0,1 (With LAN)

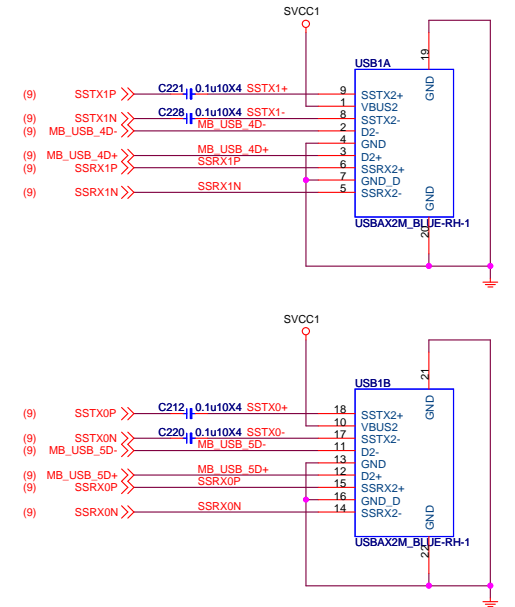
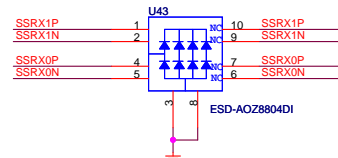
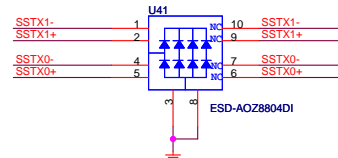
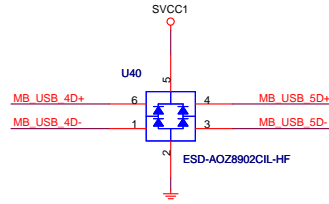
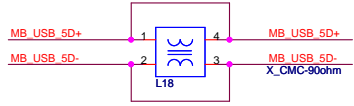
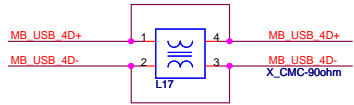
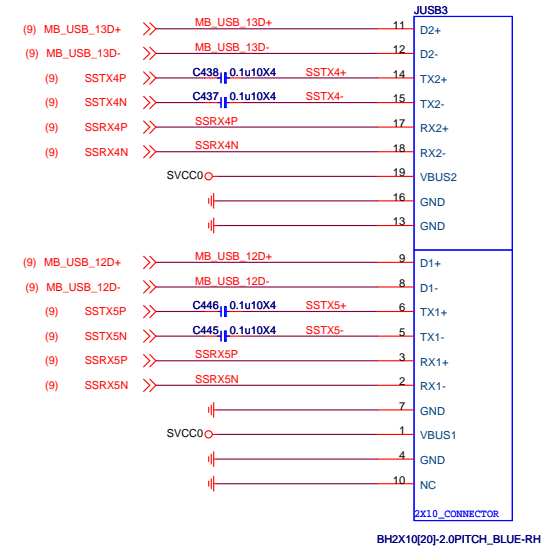
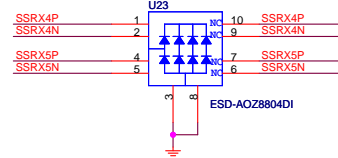
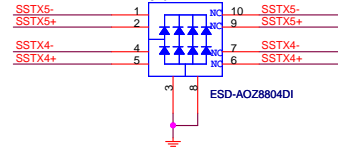
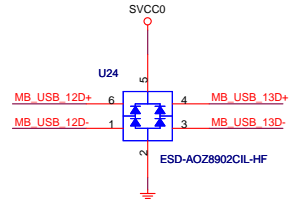
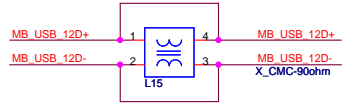
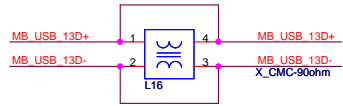


FRONT USB PORT 8,9



FRONT USB PORT 10,11

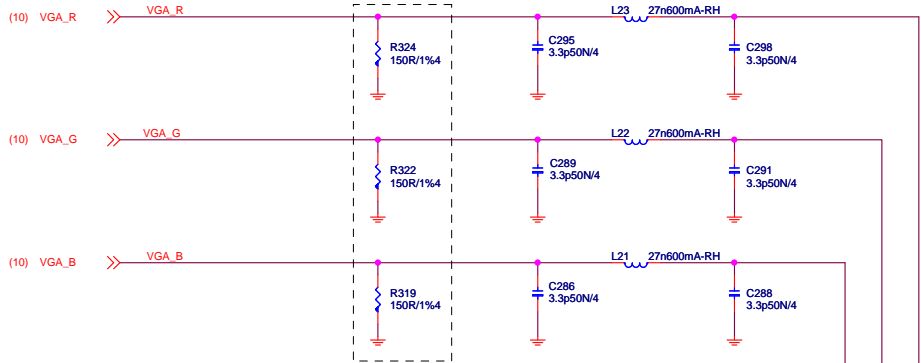
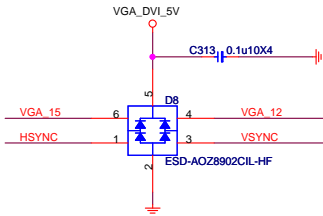
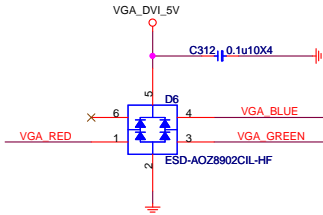
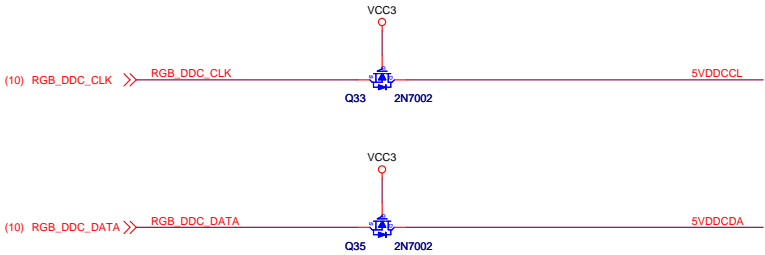
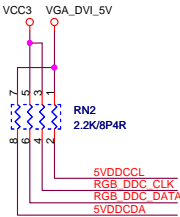




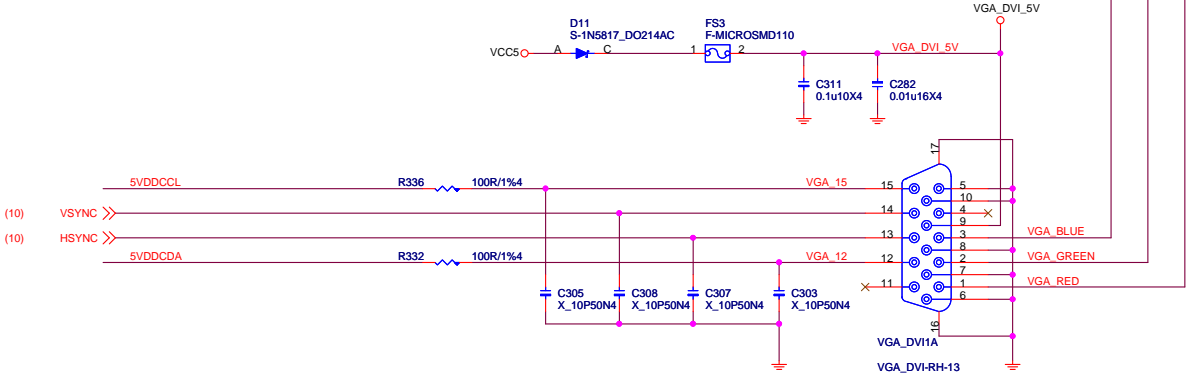
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN

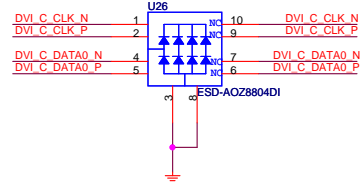


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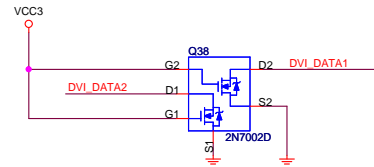
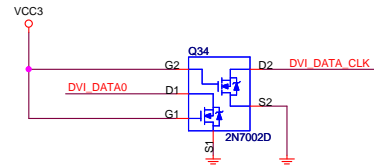
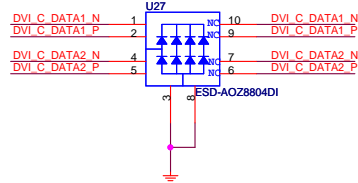
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

(3) DVI_DDPB_CLK_N << DVI_DDPB_CLK_N C337 0.1u10X4 DVI_C_CLK_N R498 680R/4
 (3) DVI_DDPB_CLK_P << DVI_DDPB_CLK_P C336 0.1u10X4 DVI_C_CLK_P R524 680R/4
 (3) DVI_DDPB_TXN0 << DVI_DDPB_TXN0 C362 0.1u10X4 DVI_C_DATA0_N R493 680R/4
 (3) DVI_DDPB_TXP0 << DVI_DDPB_TXP0 C361 0.1u10X4 DVI_C_DATA0_P R507 680R/4
 (3) DVI_DDPB_TXN1 << DVI_DDPB_TXN1 C338 0.1u10X4 DVI_C_DATA1_N R519 680R/4
 (3) DVI_DDPB_TXP1 << DVI_DDPB_TXP1 C339 0.1u10X4 DVI_C_DATA1_P R523 680R/4
 (3) DVI_DDPB_TXN2 << DVI_DDPB_TXN2 C364 0.1u10X4 DVI_C_DATA2_N R526 680R/4
 (3) DVI_DDPB_TXP2 << DVI_DDPB_TXP2 C363 0.1u10X4 DVI_C_DATA2_P R514 680R/4

U26 AVL:D0G-05A050C-005
 D0G-06A050C-A68

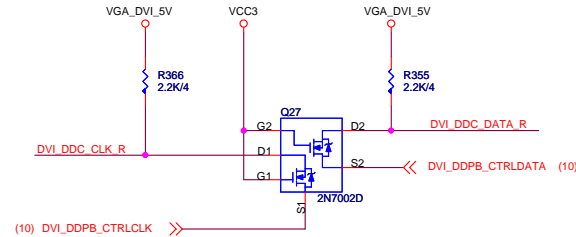
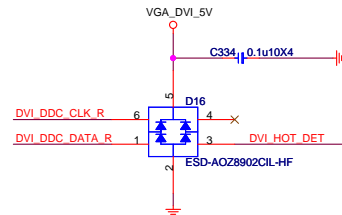
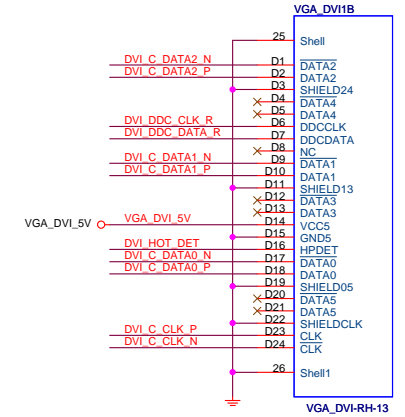


U27 AVL:D0G-05A050C-005
 D0G-06A050C-A68

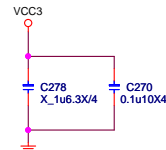
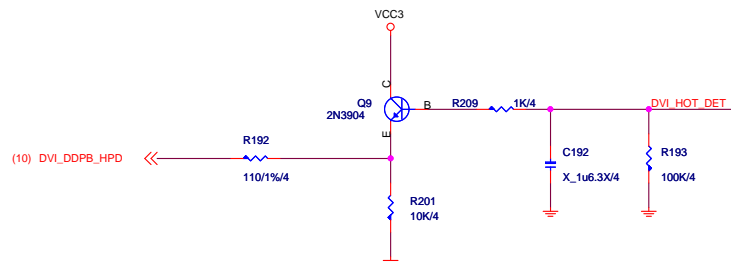


For EMI

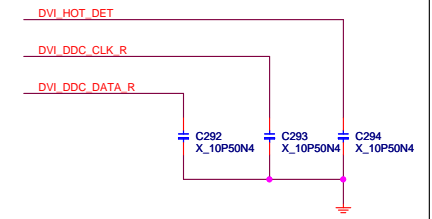
DVI_C_DATA0_N R871 X_243R/1%4
 DVI_C_DATA0_P R871 X_243R/1%4
 DVI_C_DATA1_N R874 X_243R/1%4
 DVI_C_DATA1_P R874 X_243R/1%4
 DVI_C_CLK_N R873 X_243R/1%4
 DVI_C_CLK_P R873 X_243R/1%4
 DVI_C_DATA2_N R872 X_243R/1%4
 DVI_C_DATA2_P R872 X_243R/1%4



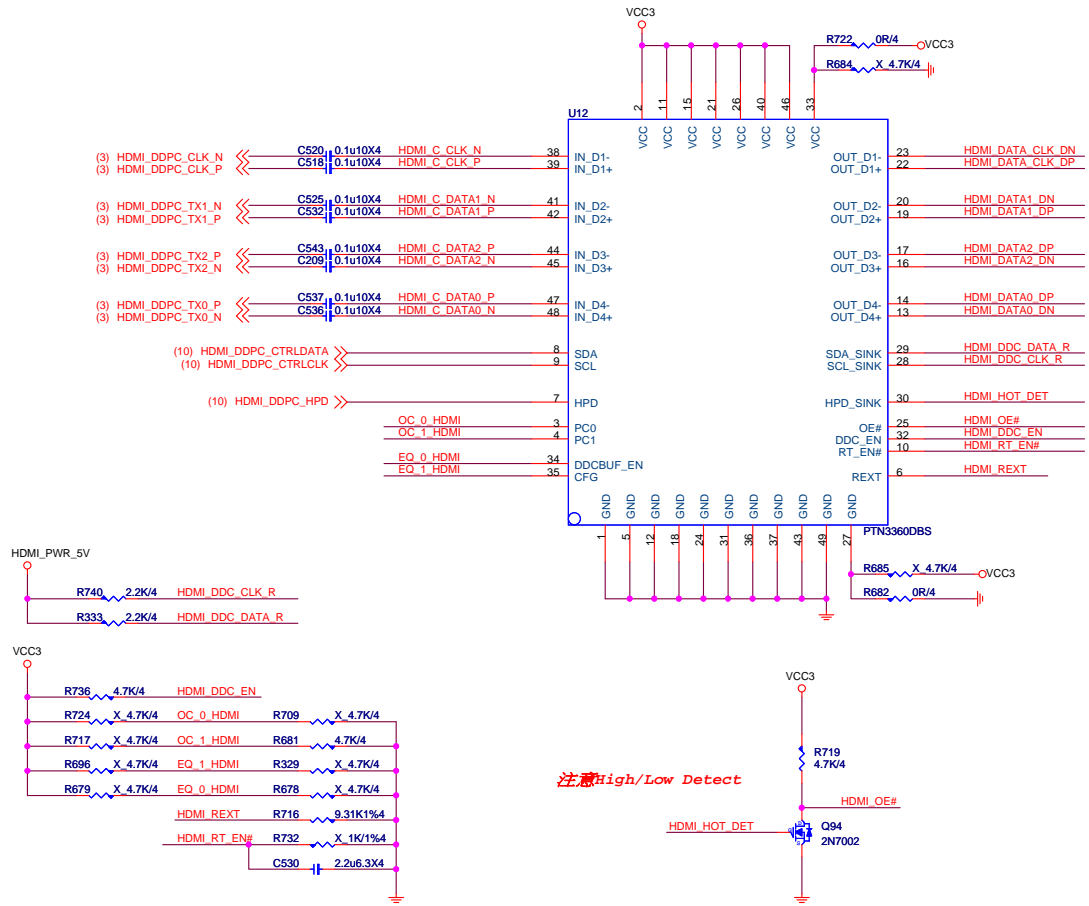
HPD



EMI



HDMI level shifter



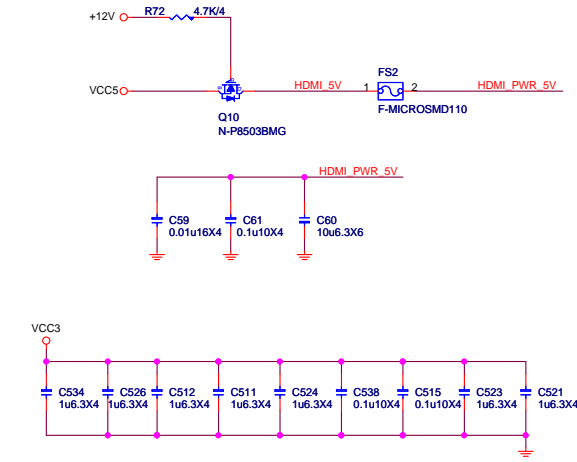
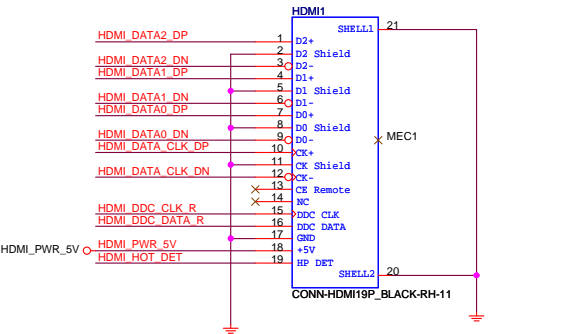
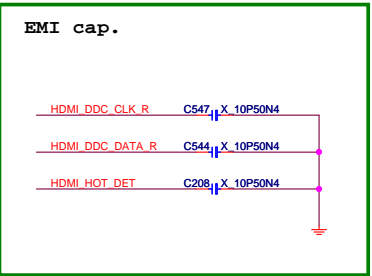
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI8_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI8_CTRL_DATA	

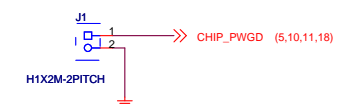
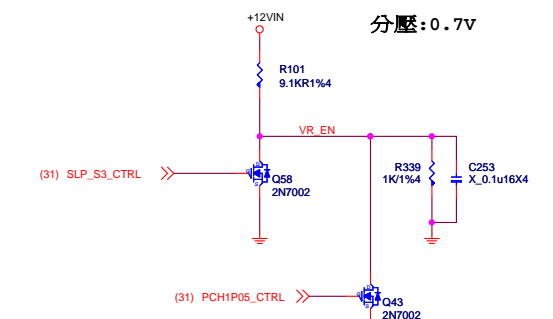
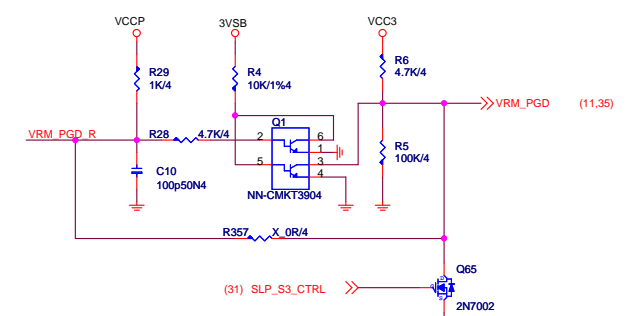
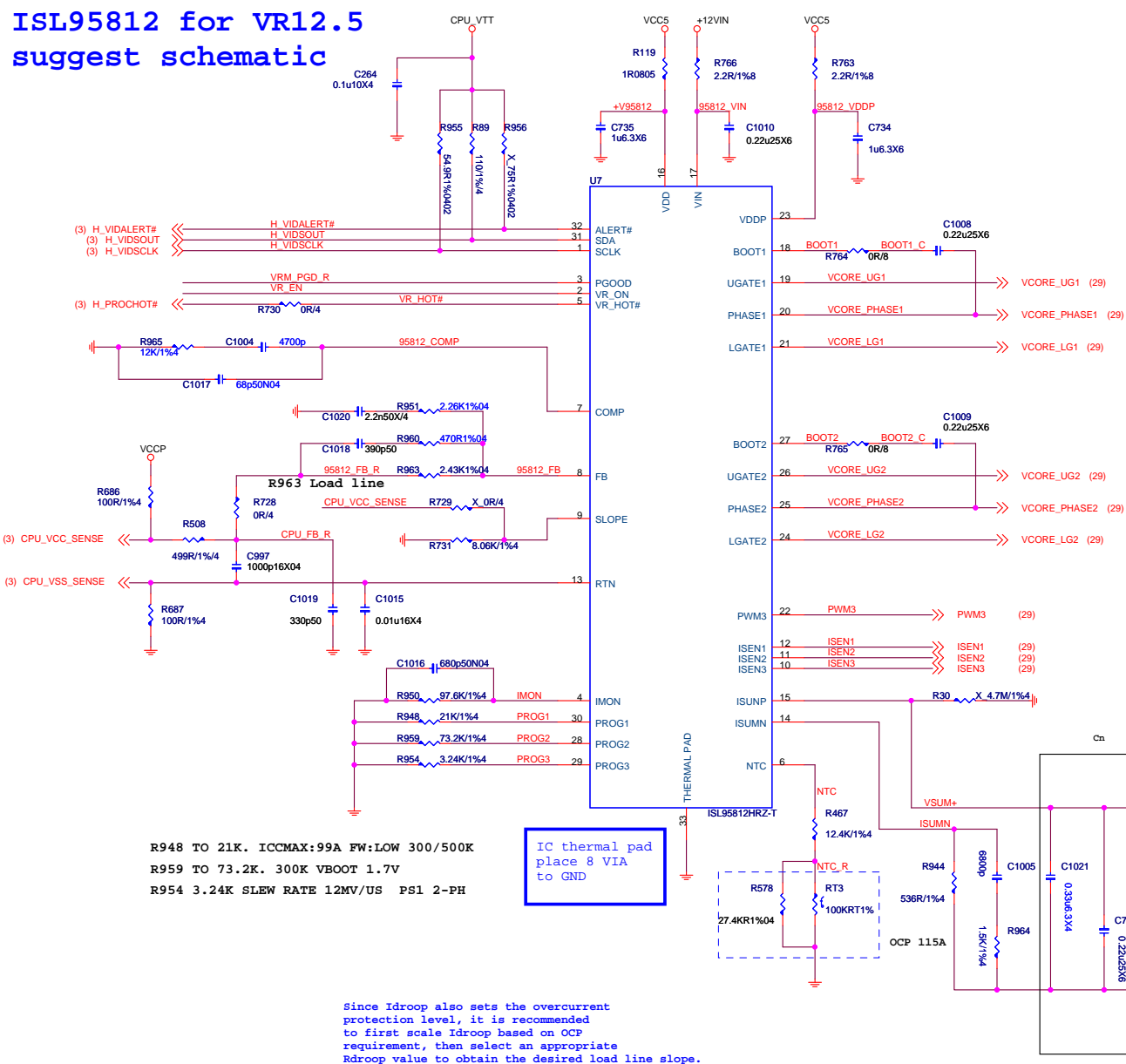


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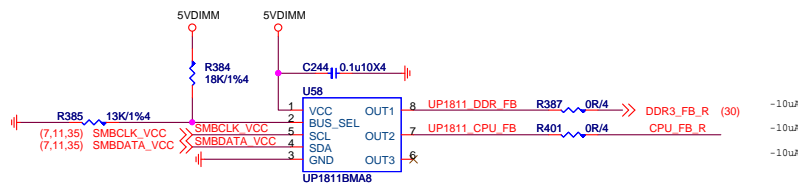
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Custom	HDMI Connector	1.1
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ISL95812 for VR12.5
suggest schematic



UPI VOLTAGE CONSOLE

0x20:RH=18K,RL=13K



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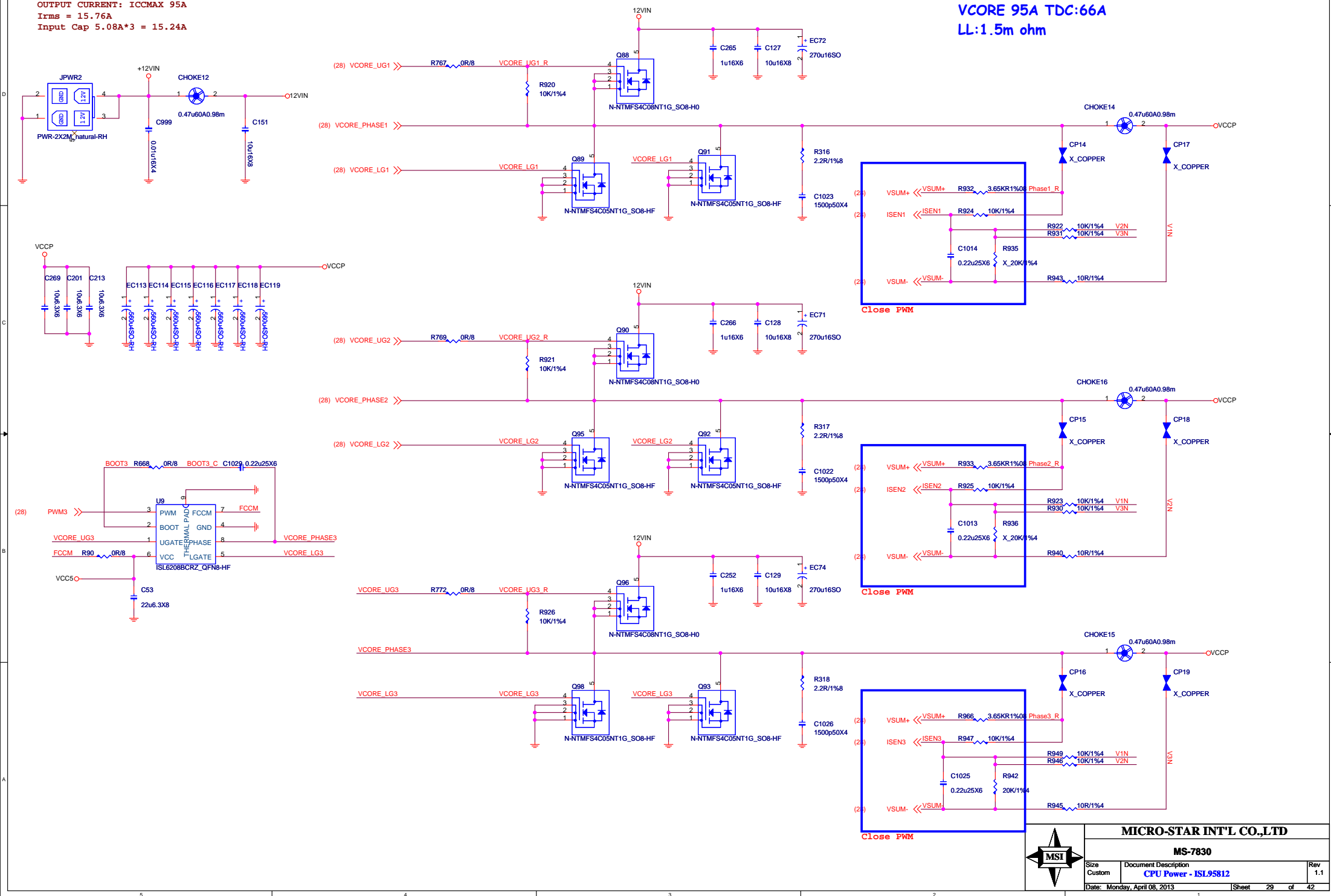
MS-7830

Size Custom	Document Description CPU Power - MOS	Rev 1.1
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Date: Monday, April 08, 2013	Sheet 28 of 42
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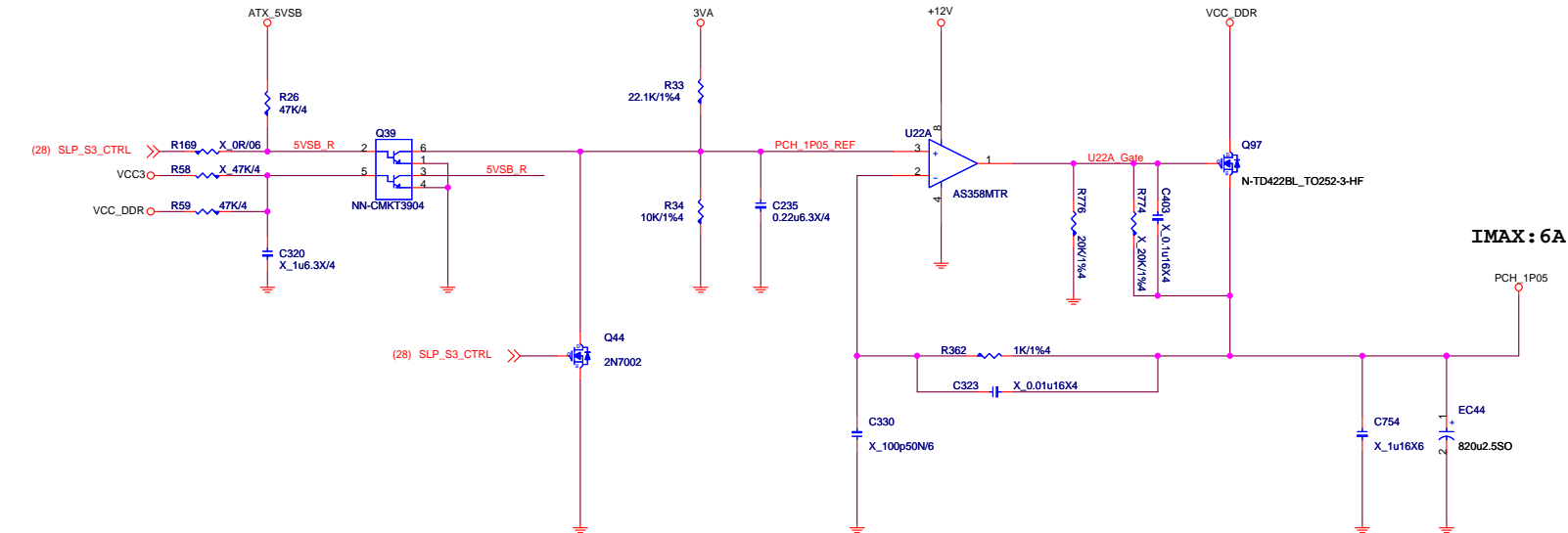
OUTPUT CURRENT: ICCMAX 95A
 Irms = 15.76A
 Input Cap 5.08A*3 = 15.24A

Vcore 95A TDC:66A
 LL:1.5m ohm

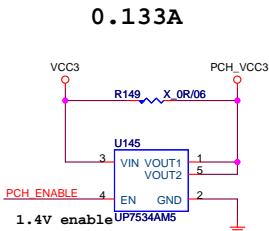


MICRO-STAR INT'L CO.,LTD			
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Size	Document Description	Rev	
Custom	CPU Power - ISL95812	1.1	
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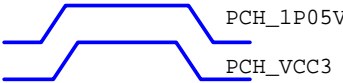
PCH Power:1.05V
PCH Core 6A



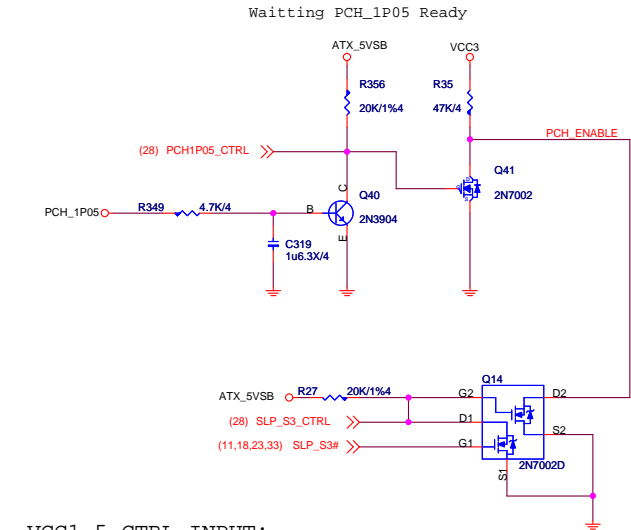
PCH Power:3.3V



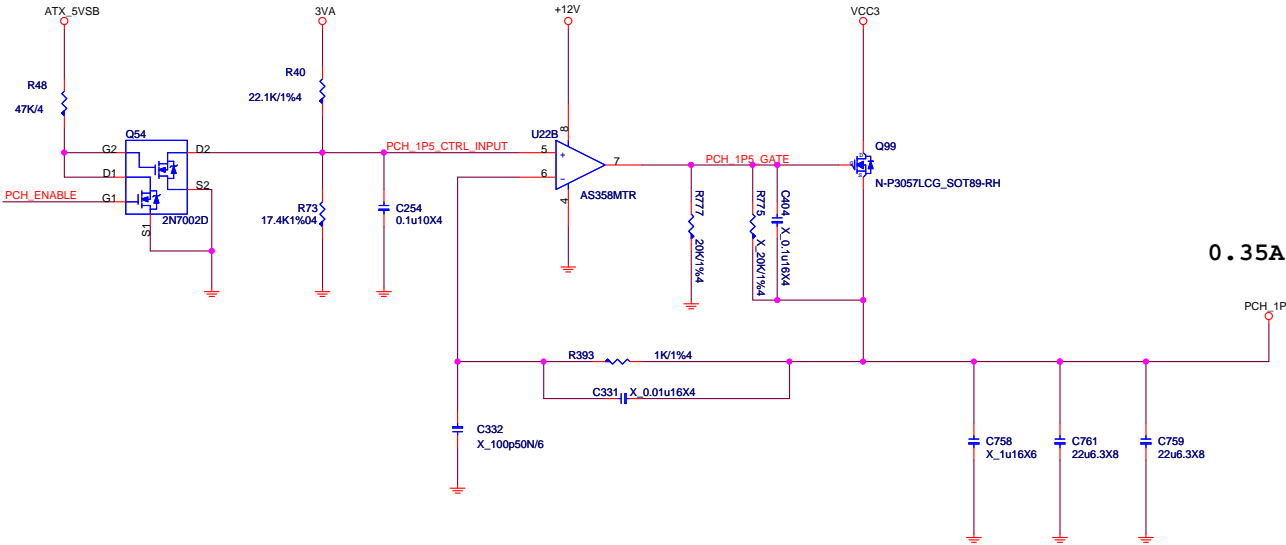
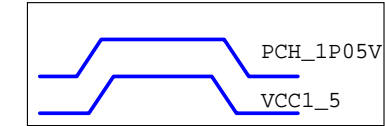
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



PCH Power:1.5V

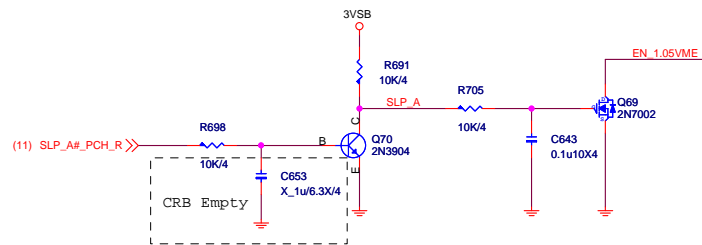


VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



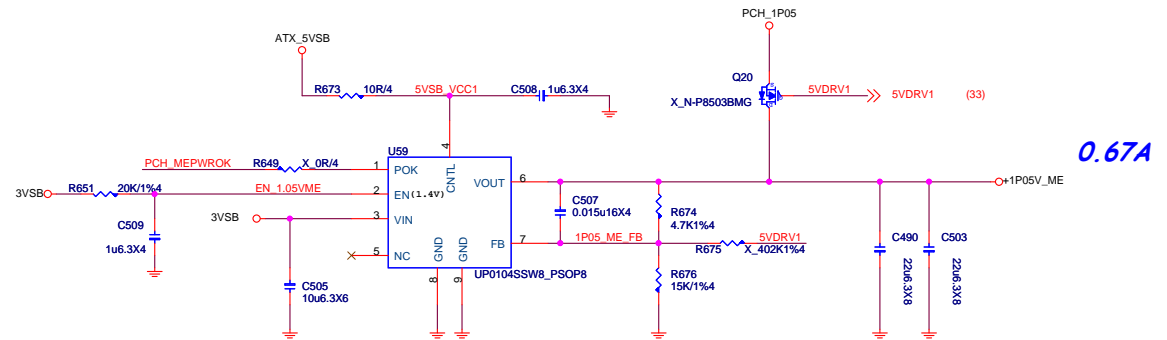
MICRO-STAR INT'L CO.,LTD			
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Custom	PCH Power - OP+MOS	1.1	
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SLP_A

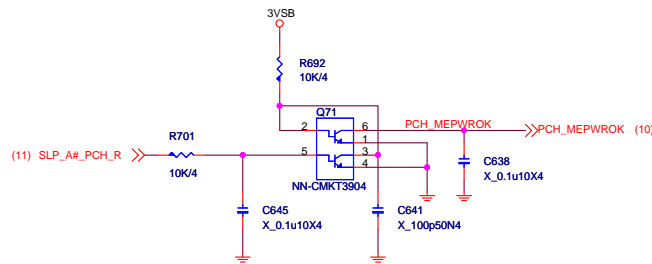
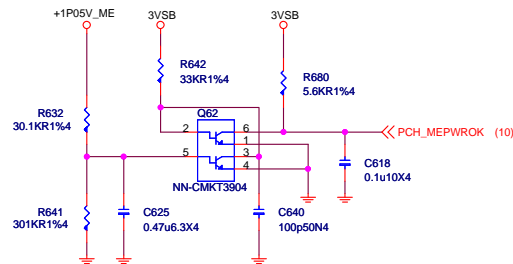


ME Power Control

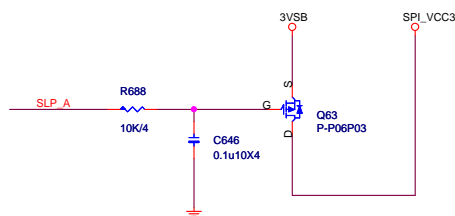
+1.05V_ME(VCCIO_ME)



PCH_MEPWROK



+3.3V_ME



ME Power for SPI rom

VCC3 — R700 — X_0R/06 — SPI_VCC3

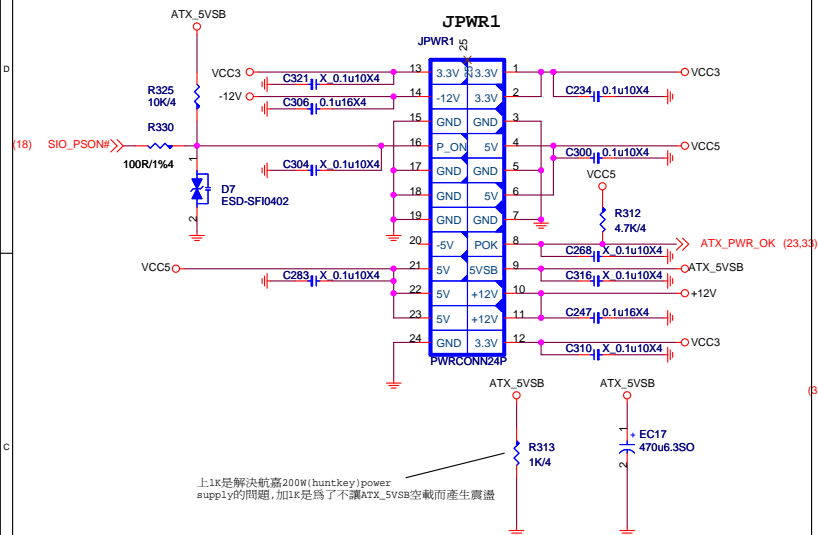


MICRO-STAR INT'L CO.,LTD

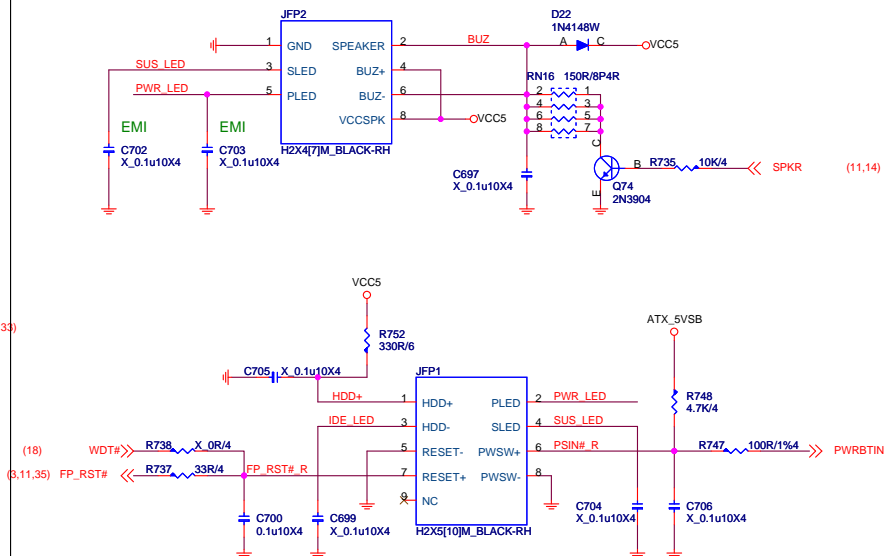
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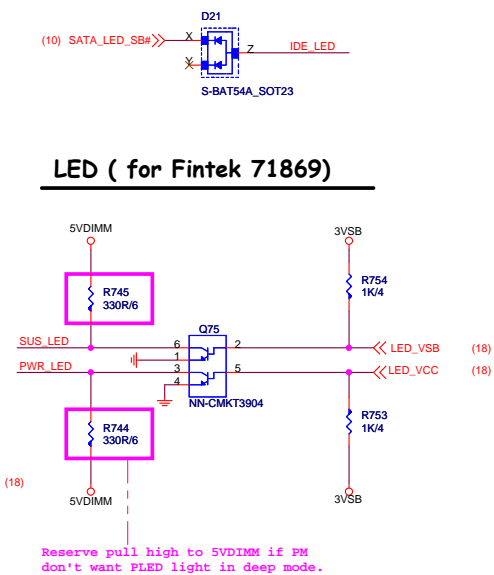
ATX POWER CONNECTOR



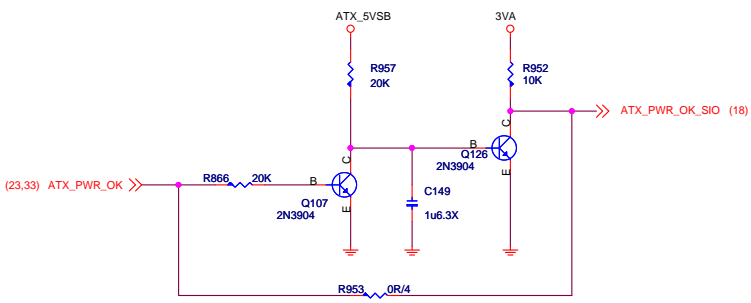
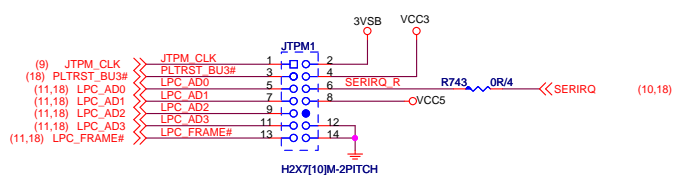
FRONT PANEL



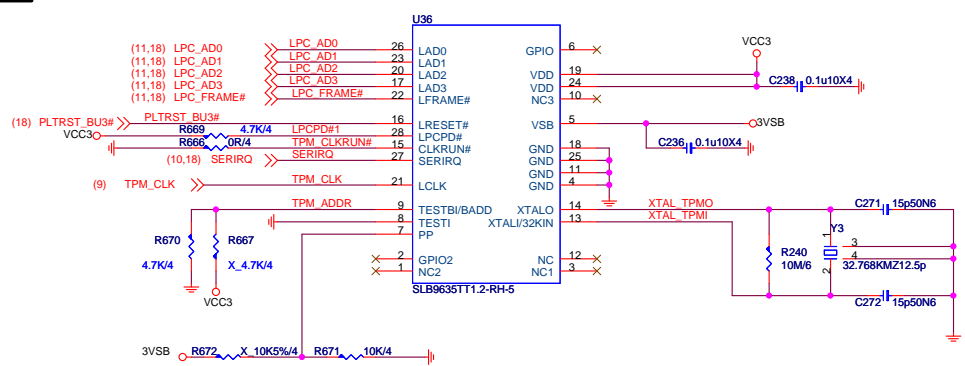
LED (for Fintek 71869)



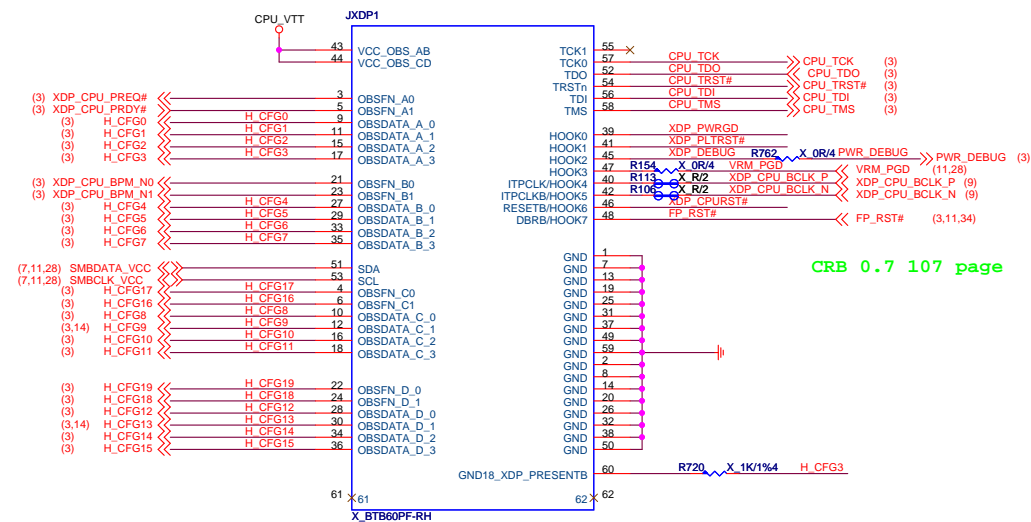
TPM



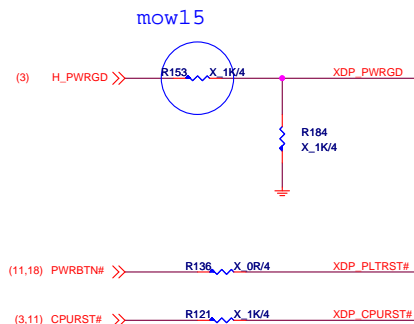
On Board TPM



Reserve debug port 5020

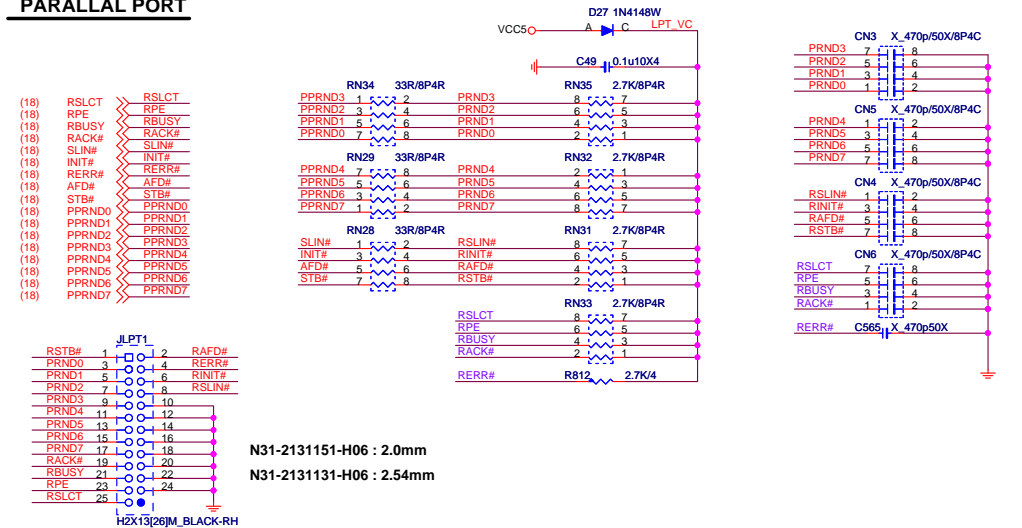


CRB 0.7 107 page

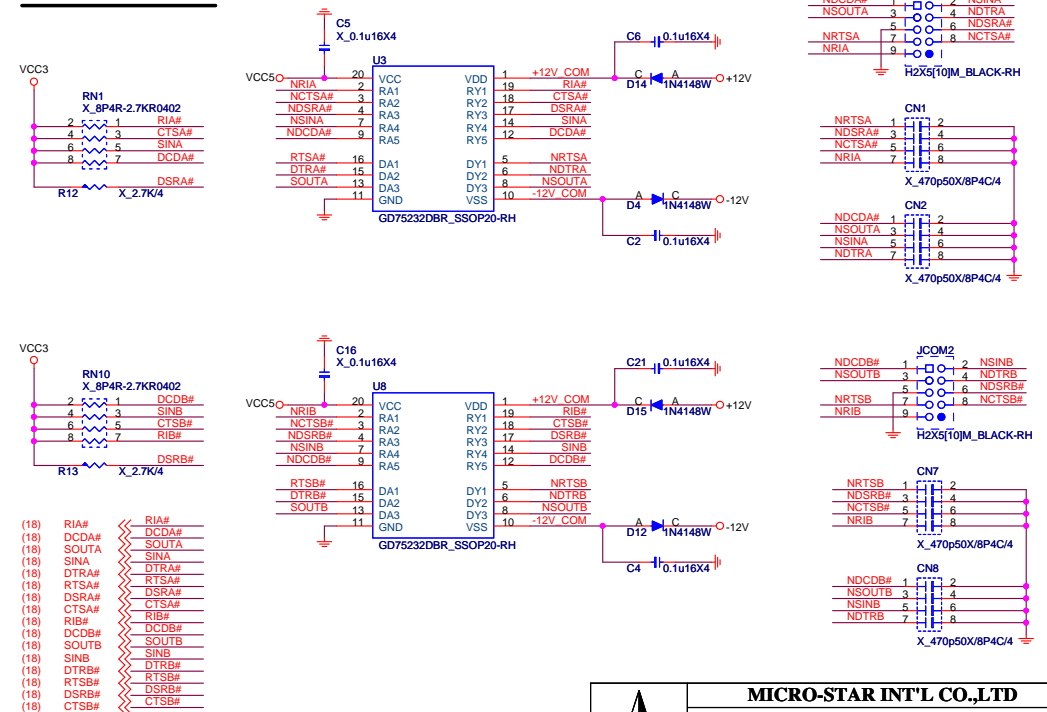


PLACE NEAR XDP CONNECTOR

PARALLAL PORT



SERIAL PORT 1&2

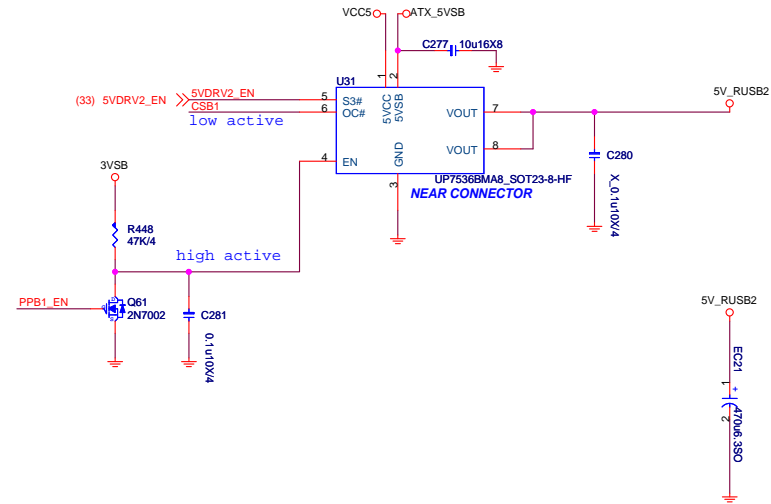
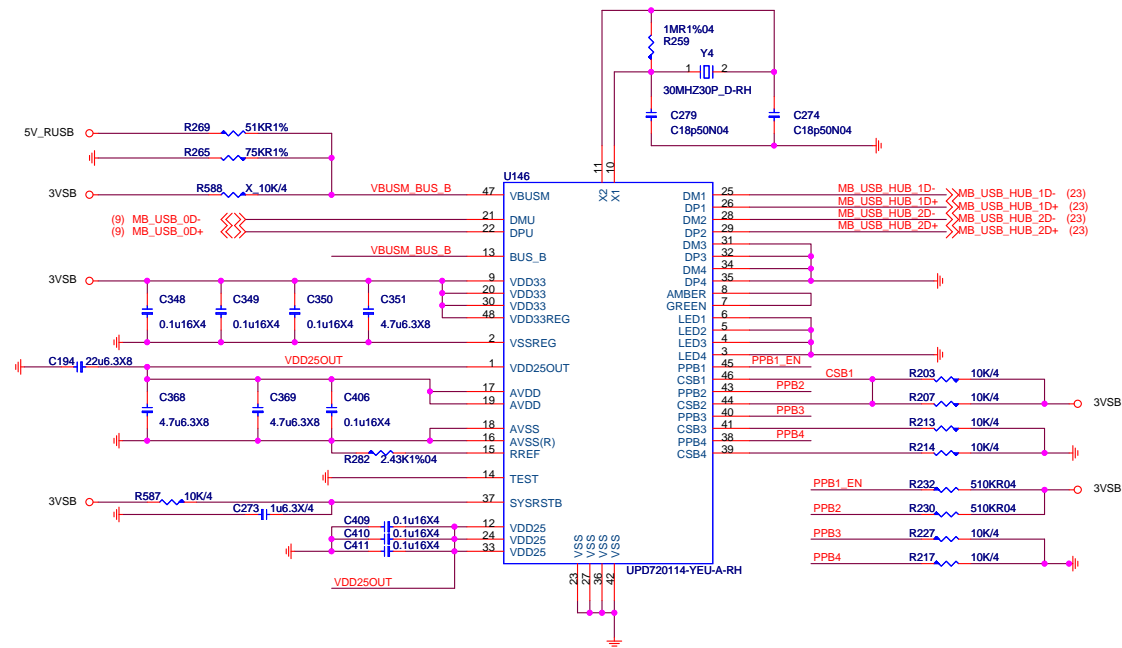


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USB HUB



EMI CAP solution

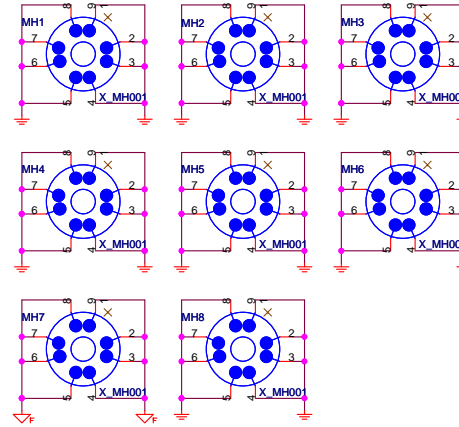


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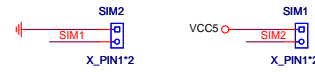
D1000
LAN
2N7002

如果用料選用Vth < 1V ,請統一選擇這兩顆料 D03-0341409-A68 / D03-0230019-A30

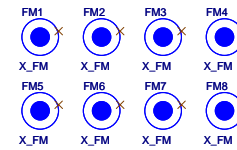
Mounting Holes



Simulation



Optical Fiducial Marks-120



Test point

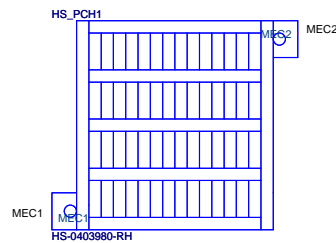
VCCP		CPU_VCCIN
CPU_VTT		CPU_VCCIO
VCC_DDR		VCC_DDR
VTT_DDR		VTT_DDR
PCH_1P05		PCH_CORE
PCH_1P5		PCH_VCCVRM
PCH_VCC3		PCH_VCC3
5VDIMM		5VDIMM
3VSB		3VSB
VBAT		VBAT
3VA		3VA

LA4
Label
501~7830-XXX
MKT-LABEL

HDMI_RLA1
Real Label
HDMI
HDMI_RLA

LABEL2
MKT
X_BUY

HEATSINK



PCB1
7830_11

HDMI_LA1
Label
HDMI
HDMI_LABEL

CPU_H1
CPU
鐵座
CPU_H1

LA3
AMI_BIOS
LABEL
BIOS_LABEL

BAT1_X1
BAT-BCR2032P-RH

PK0-0783011-G37, 精成, 23, 寶安恩斯邁廠 (MSIS)
PK0-0783011-G37, 精成, 2, 寶安恩斯邁廠 (MSIS)
PK0-0783011-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)
PK0-0783011-E48, 競華, 2, 寶安恩斯邁廠 (MSIS)

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